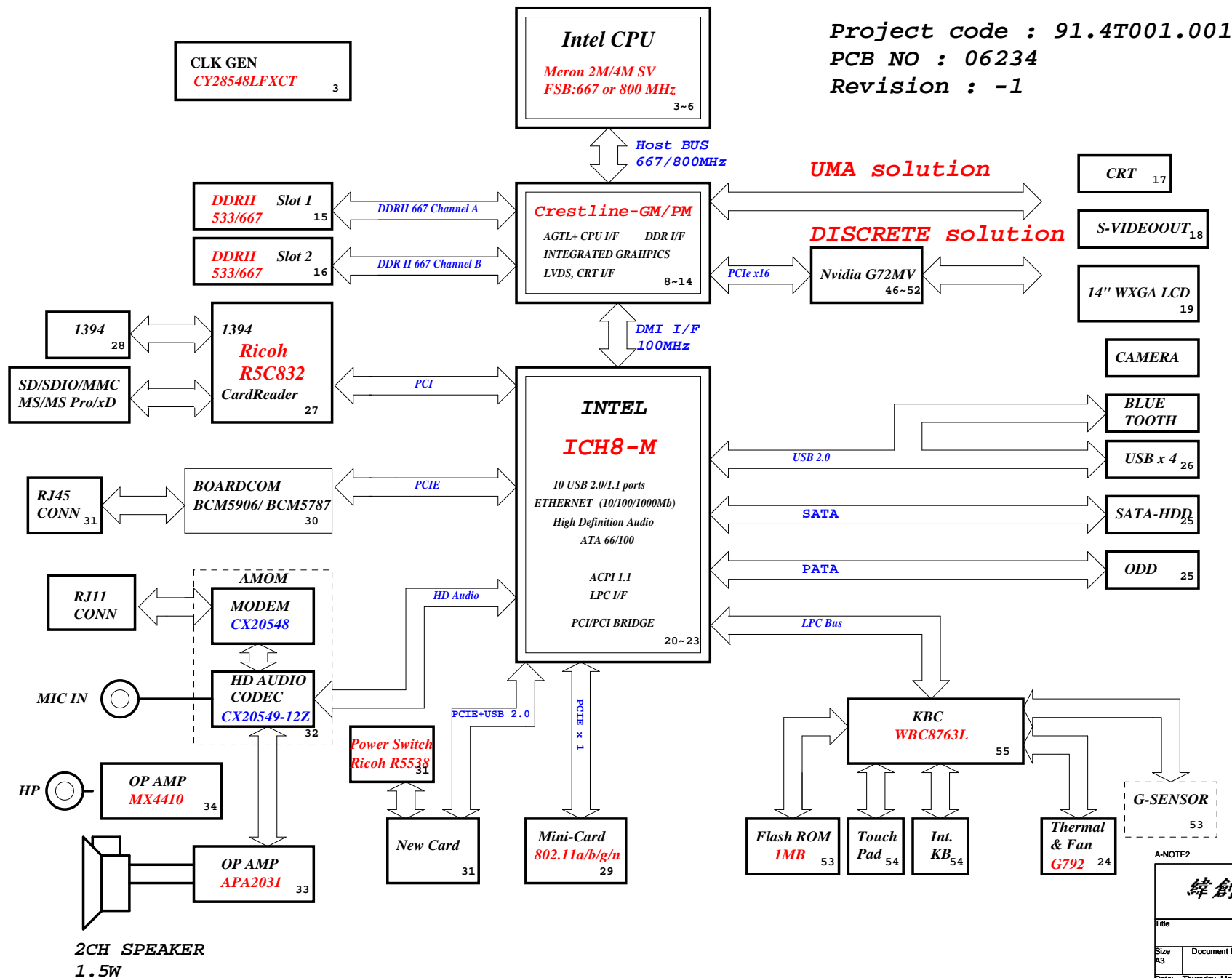


Anote2.0 Block Diagram



SYSTEM DC/DC TPS51120 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3D3V_S5
SYSTEM DC/DC ISL6268CAZ 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
SYSTEM DC/DC TPS51116 40	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 0D9V_S0
CHARGER ISL6255	
INPUTS	OUTPUTS
DCBATOUT	BT+ 20V 3.0A 5V 100mA
CPU DC/DC ISL6262ACRZ 36,37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1: Signal 1	
L2: VCC	
L3: Signal 2	
L4: Signal 3	
L5: GND	
L6: Signal 4	

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Block Diagram		
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCLI_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCLI_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCLI_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCLI_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port config bit1

A16 swap override strap		
PCI_GNT3#	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT0#	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
Integrated VccSus1_05,VccSus1_5,VccCLI_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLAN1_05VccCLI_05		
LAN100_SLP	High=Enable	Low=Disable

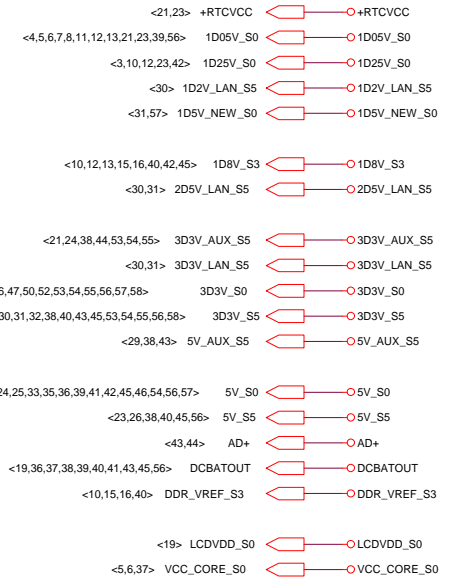
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



INTEL CRESTLINE STRAP PIN

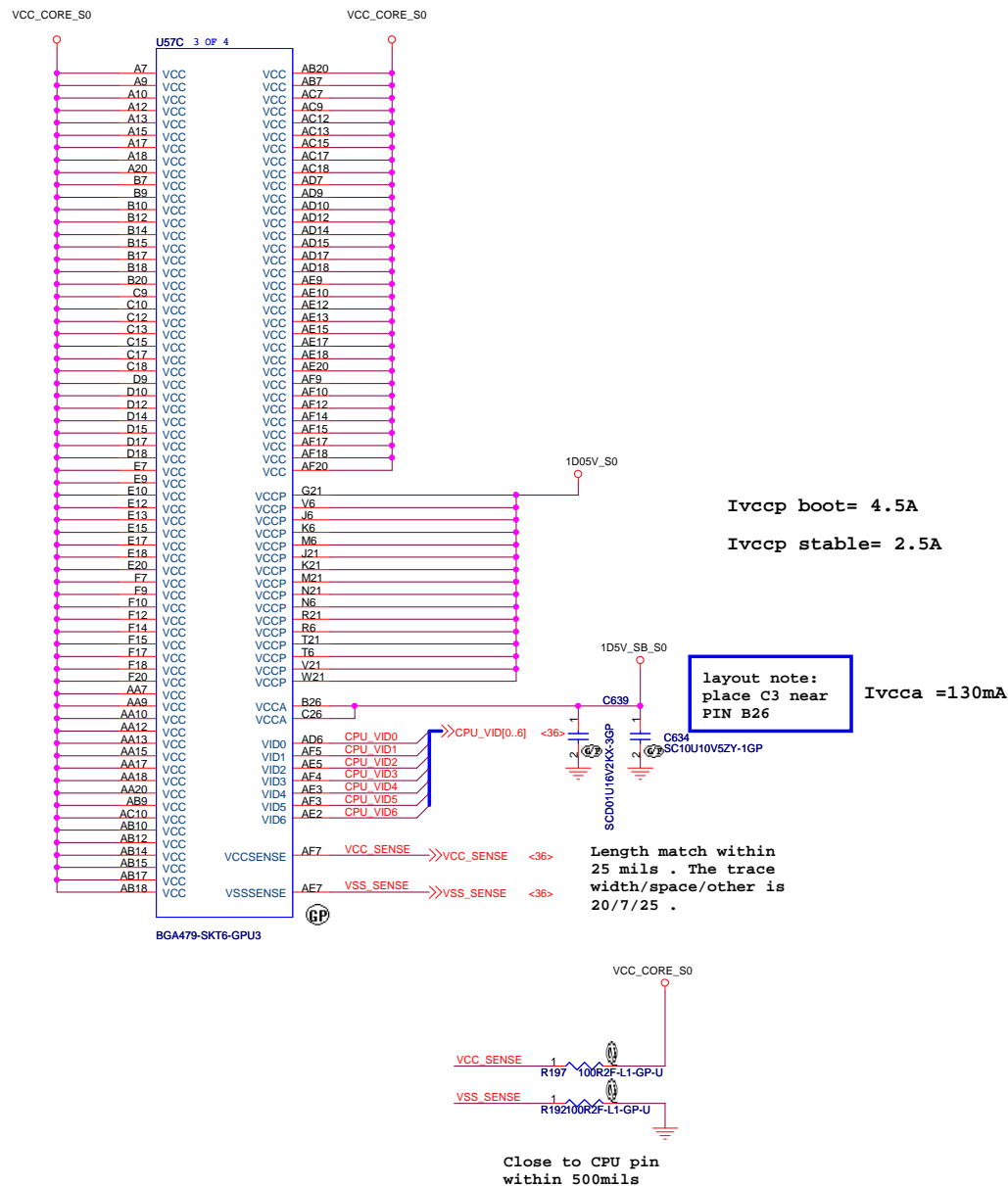
CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled★
CFG 19 DMI Lane Reserved	Normal Operation★	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation★	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HL(11)	Normal Operation	

A-NOTE2

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
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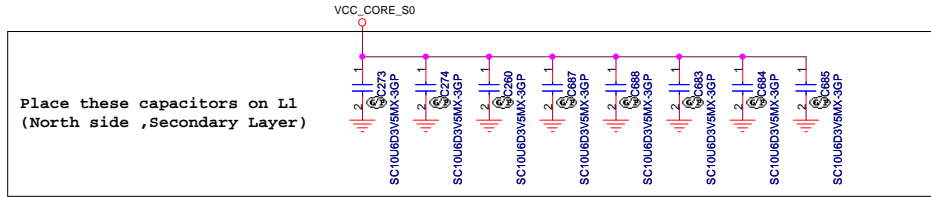
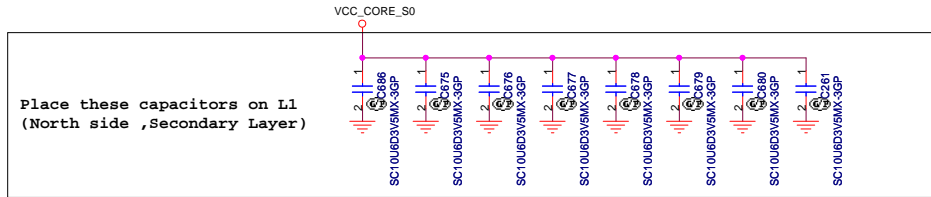
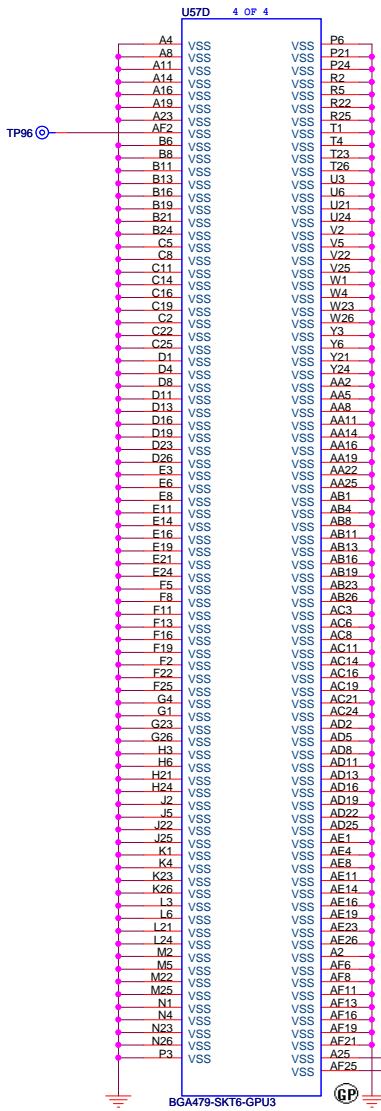




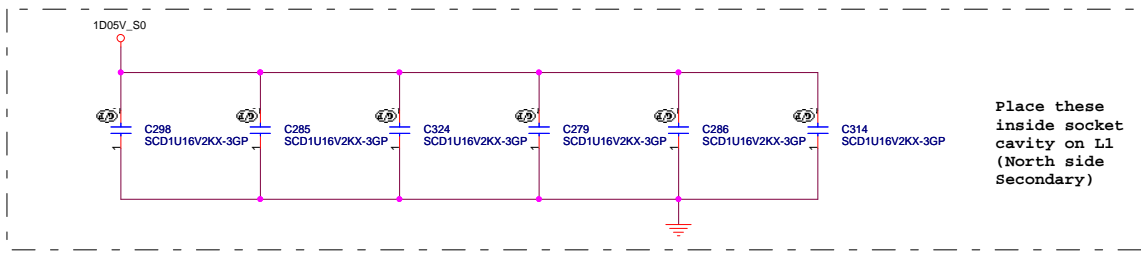
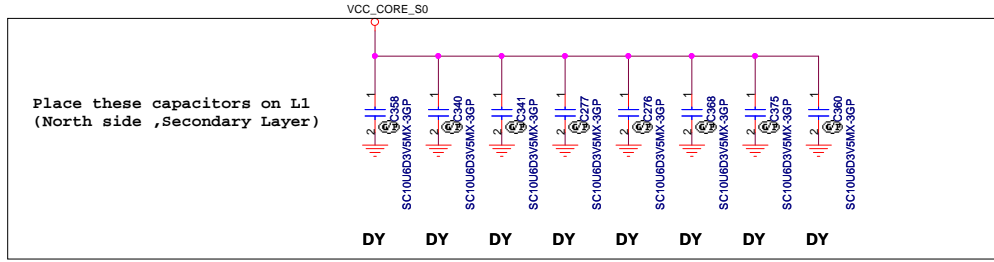
A-NOTE2

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Title	
Merom(2/3)-AGTL+/PWR	
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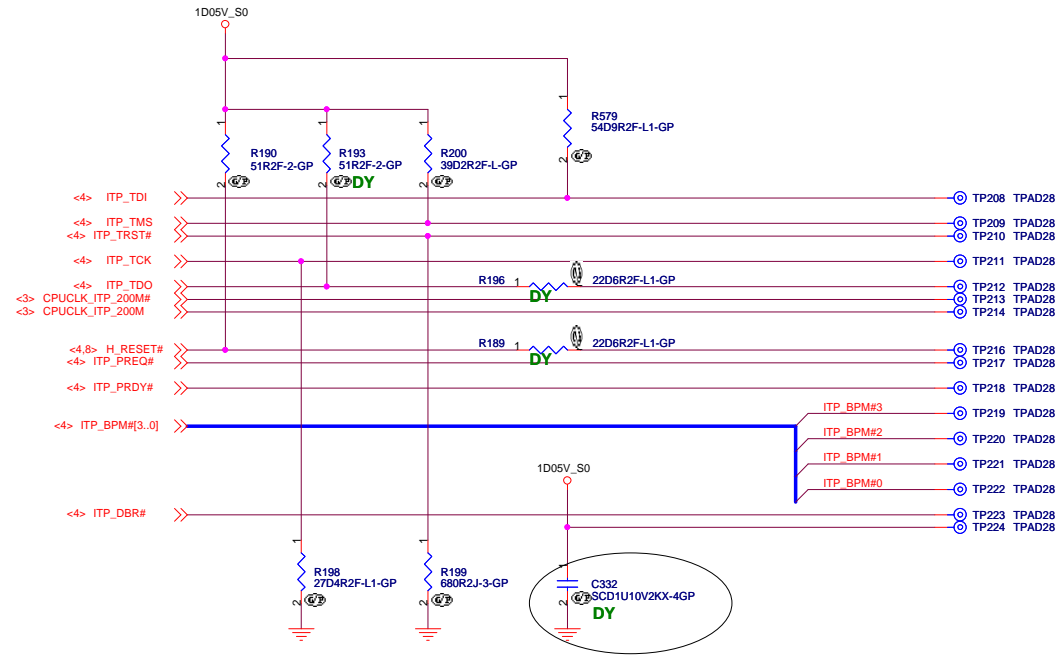


Mid Freqeuncd Decoupling



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Title			
Meron(3/3)-GND&Bypass			
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ITP Connector

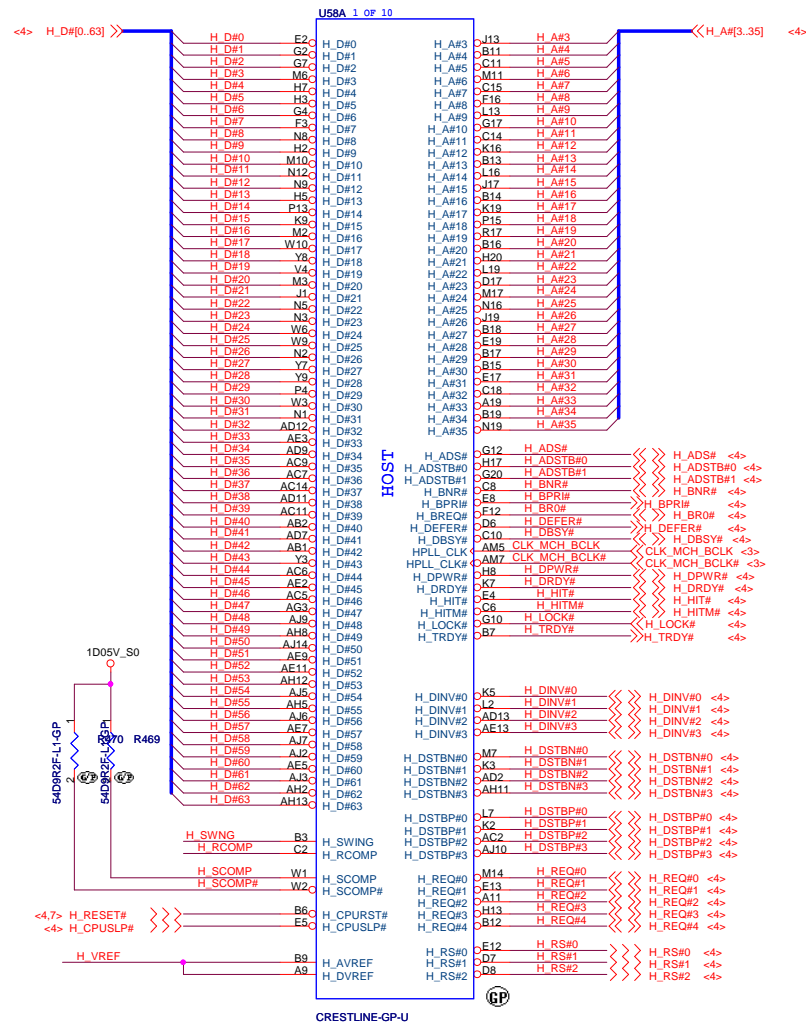
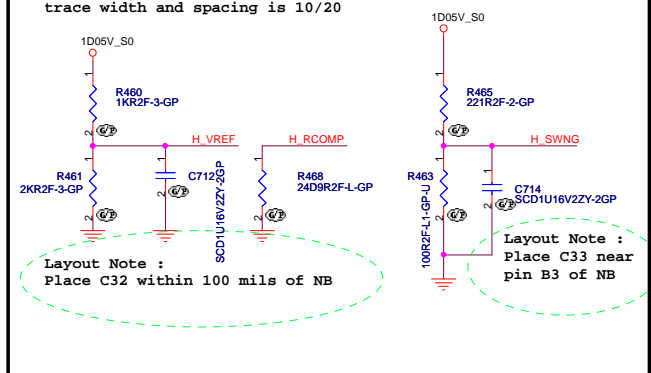


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Title			
Meron(3/3)-GND&Bypass			
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layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



A-NOTE2

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Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(1/7)-AGTL+/DM/DDR2

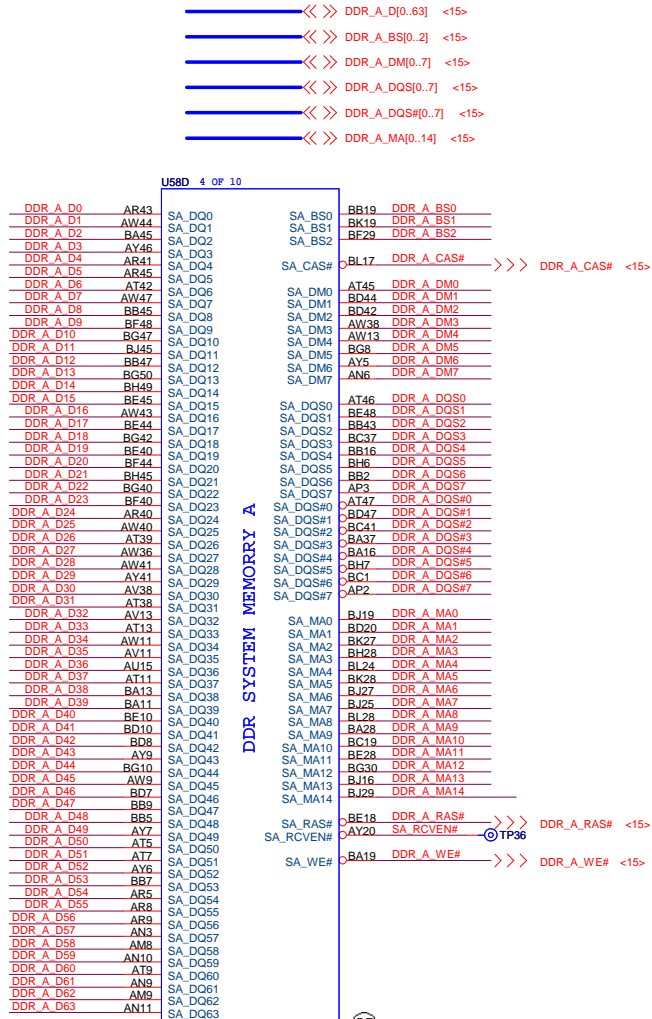
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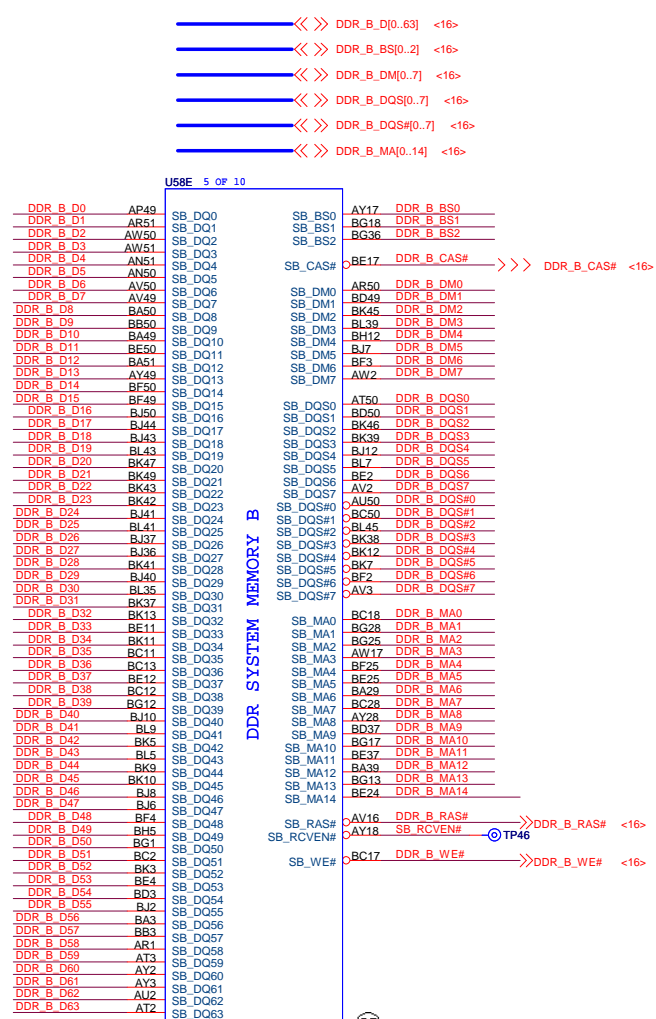
Rev
-1



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DDR SYSTEM MEMORY A

CRESTLINE-GP-U



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DDR SYSTEM MEMORY B

CRESTLINE-GP-U



A-NOTE2

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Title			
CRESTLINE(2/7)-DDR2 A/B CH			
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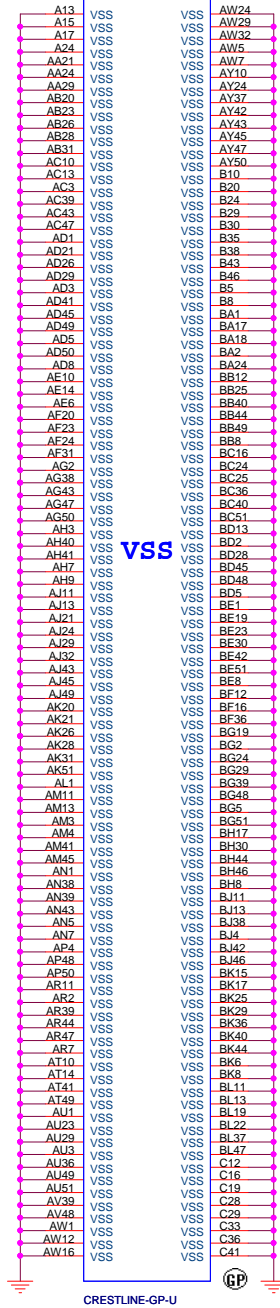
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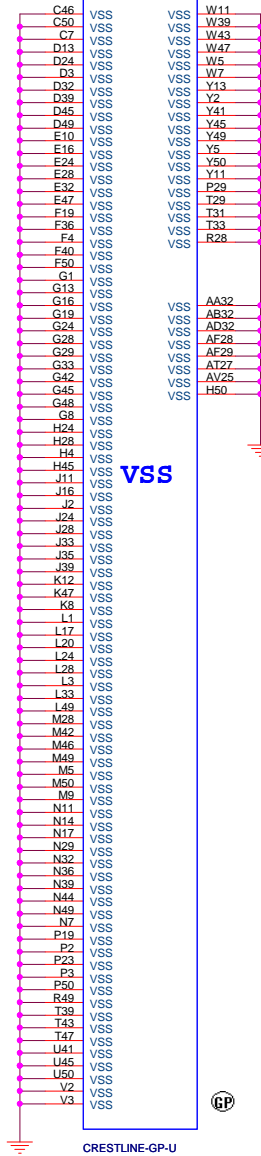
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CRESTLINE-GP-U

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CRESTLINE-GP-U

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Title	
CRESTLINE(7/7)-PWR/GND	
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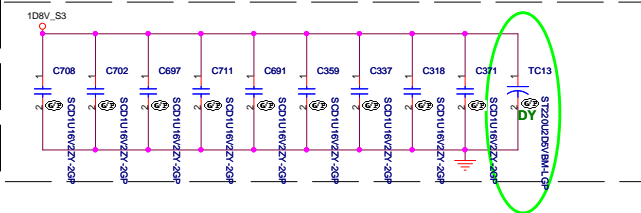
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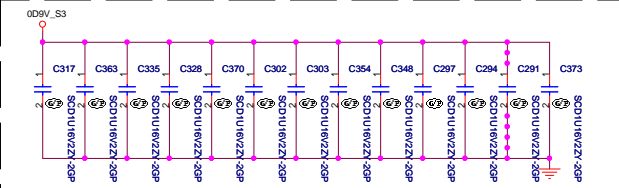
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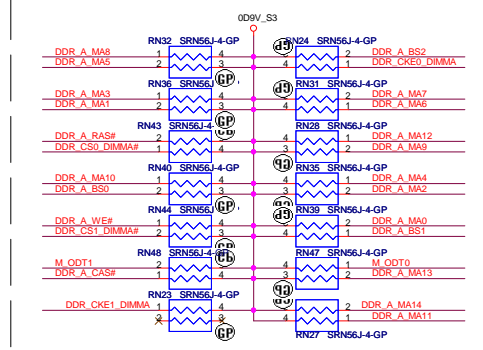
Layout Note:
Place near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM1,all trace length Max=1.5"



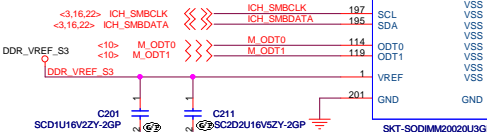
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DDR A MA1	101	A1	DDR A DQS1	31	DDR A DQS1
DDR A MA2	100	A2	DDR A DQS2	51	DDR A DQS2
DDR A MA3	99	A3	DDR A DQS3	70	DDR A DQS3
DDR A MA4	98	A4	DDR A DQS4	131	DDR A DQS4
DDR A MA5	97	A5	DDR A DQS5	148	DDR A DQS5
DDR A MA6	94	A6	DDR A DQS6	169	DDR A DQS6
DDR A MA7	92	A7	DDR A DQS7	188	DDR A DQS7
DDR A MA8	93	A8	DDR A DQS8	211	DDR A DQS8
DDR A MA9	91	A9	DDR A DQS9	229	DDR A DQS9
DDR A MA10	105	A10/AP	DDR A DQS10	249	DDR A DQS10
DDR A MA11	90	A11	DDR A DQS11	268	DDR A DQS11
DDR A MA12	89	A12	DDR A DQS12	289	DDR A DQS12
DDR A MA13	116	A13	DDR A DQS13	312	DDR A DQS13
DDR A MA14	86	A14	DDR A DQS14	336	DDR A DQS14
DDR A BS2	84	A15	DDR A DQS15	366	DDR A DQS15
	85	A16,BA2			

DDR A BS0	107	BA0	DDR A DM0	10	DDR A DM0
DDR A BS1	106	BA1	DDR A DM1	26	DDR A DM1
DDR A D0	7	DQ0	DDR A DM2	62	DDR A DM2
DDR A D1	5	DQ1	DDR A DM3	67	DDR A DM3
DDR A D2	17	DQ2	DDR A DM4	130	DDR A DM4
DDR A D3	19	DQ3	DDR A DM5	147	DDR A DM5
DDR A D4	6	DQ4	DDR A DM6	170	DDR A DM6
DDR A D5	14	DQ5	DDR A DM7	185	DDR A DM7
DDR A D6	16	DQ6			
DDR A D7	23	DQ7	M_CLK_DDR0	30	M_CLK_DDR0
DDR A D8	25	DQ8	M_CLK_DDR#0	32	M_CLK_DDR#0
DDR A D9	35	DQ9	M_CLK_DDR1	154	M_CLK_DDR1
DDR A D10	37	DQ10	M_CLK_DDR#1	166	M_CLK_DDR#1
DDR A D11	20	DQ11			
DDR A D12	22	DQ12			
DDR A D13	38	DQ13			
DDR A D14	45	DQ14			
DDR A D15	55	DQ15			
DDR A D16	57	DQ16			
DDR A D17	44	DQ17			
DDR A D18	46	DQ18			
DDR A D19	56	DQ19			
DDR A D20	61	DQ20			
DDR A D21	63	DQ21			
DDR A D22	73	DQ22			
DDR A D23	62	DQ23			
DDR A D24	74	DQ24			
DDR A D25	76	DQ25			
DDR A D26	123	DQ26			
DDR A D27	125	DQ27			
DDR A D28	135	DQ28			
DDR A D29	137	DQ29			
DDR A D30	124	DQ30			
DDR A D31	126	DQ31			
DDR A D32	134	DQ32			
DDR A D33	136	DQ33			
DDR A D34	141	DQ34			
DDR A D35	143	DQ35			
DDR A D36	151	DQ36			
DDR A D37	153	DQ37			
DDR A D38	140	DQ38			
DDR A D39	152	DQ39			
DDR A D40	154	DQ40			
DDR A D41	157	DQ41			
DDR A D42	159	DQ42			
DDR A D43	173	DQ43			
DDR A D44	175	DQ44			
DDR A D45	176	DQ45			
DDR A D46	179	DQ46			
DDR A D47	181	DQ47			
DDR A D48	189	DQ48			
DDR A D49	190	DQ49			
DDR A D50	180	DQ50			
DDR A D51	182	DQ51			
DDR A D52	192	DQ52			
DDR A D53	194	DQ53			

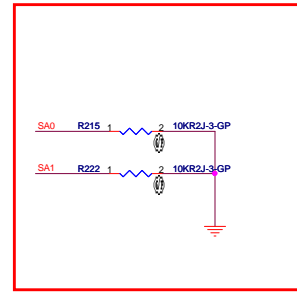
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 <9> DDR_A_CAS# <<>>
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High 5.2mm

DDR A MA0	102	A0	DDR A DQS0	13	DDR A DQS0
DDR A MA1	101	A1	DDR A DQS1	31	DDR A DQS1
DDR A MA2	100	A2	DDR A DQS2	51	DDR A DQS2
DDR A MA3	99	A3	DDR A DQS3	70	DDR A DQS3
DDR A MA4	98	A4	DDR A DQS4	131	DDR A DQS4
DDR A MA5	97	A5	DDR A DQS5	148	DDR A DQS5
DDR A MA6	94	A6	DDR A DQS6	169	DDR A DQS6
DDR A MA7	92	A7	DDR A DQS7	188	DDR A DQS7
DDR A MA8	93	A8	DDR A DQS8	211	DDR A DQS8
DDR A MA9	91	A9	DDR A DQS9	229	DDR A DQS9
DDR A MA10	105	A10/AP	DDR A DQS10	249	DDR A DQS10
DDR A MA11	90	A11	DDR A DQS11	268	DDR A DQS11
DDR A MA12	89	A12	DDR A DQS12	289	DDR A DQS12
DDR A MA13	116	A13	DDR A DQS13	312	DDR A DQS13
DDR A MA14	86	A14	DDR A DQS14	336	DDR A DQS14
DDR A BS2	84	A15	DDR A DQS15	366	DDR A DQS15
	85	A16,BA2			

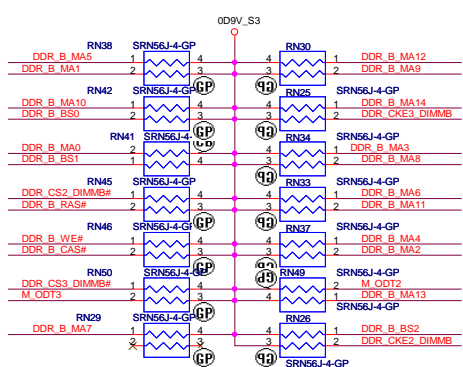
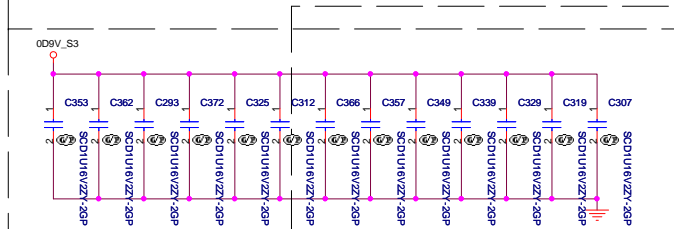


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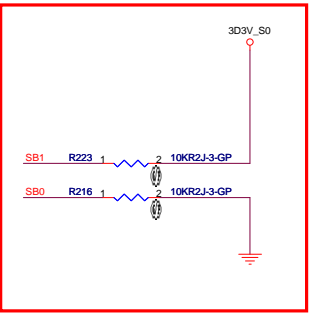
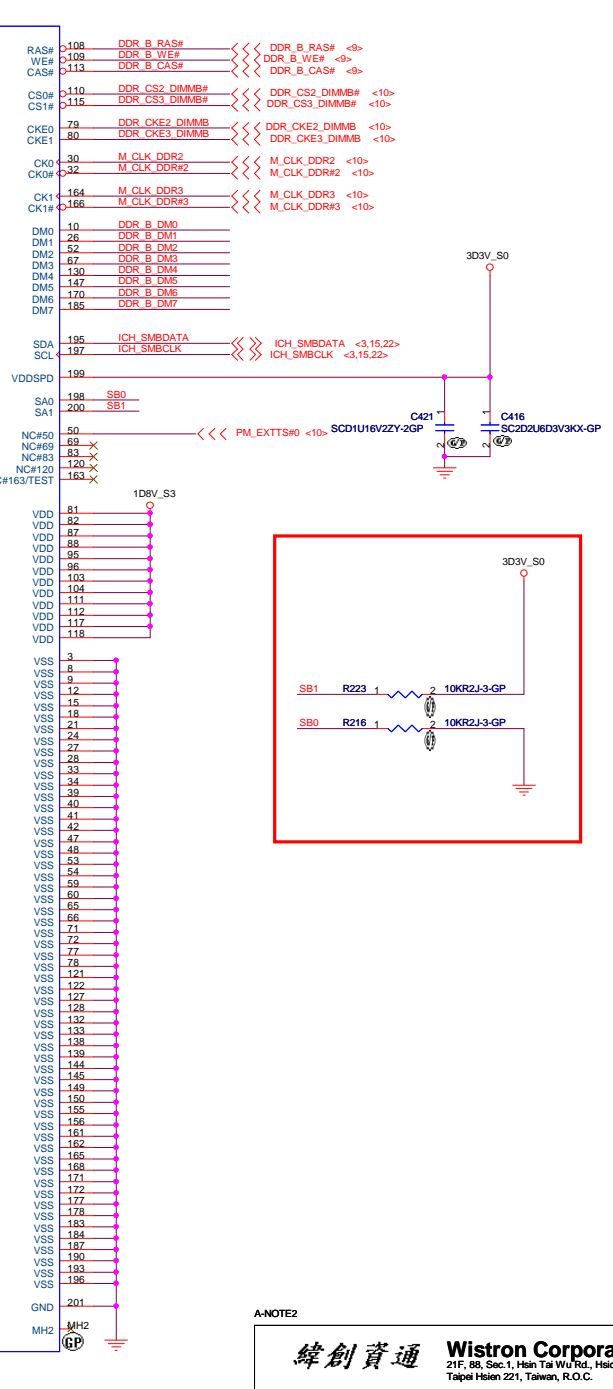
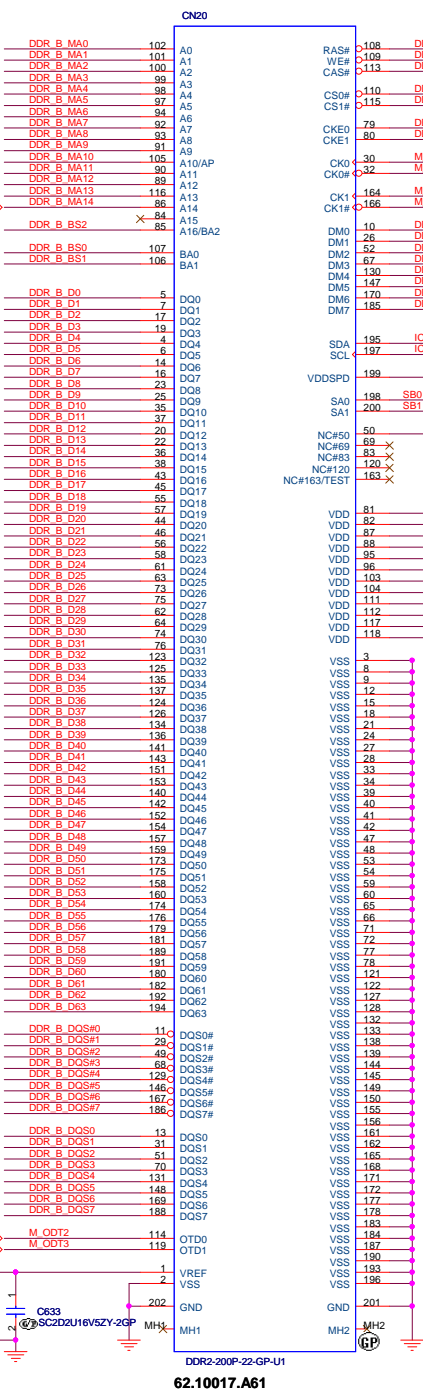
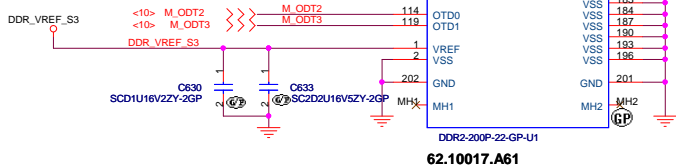
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, R.O.C.

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Customer	Anote2.0 INTEL		
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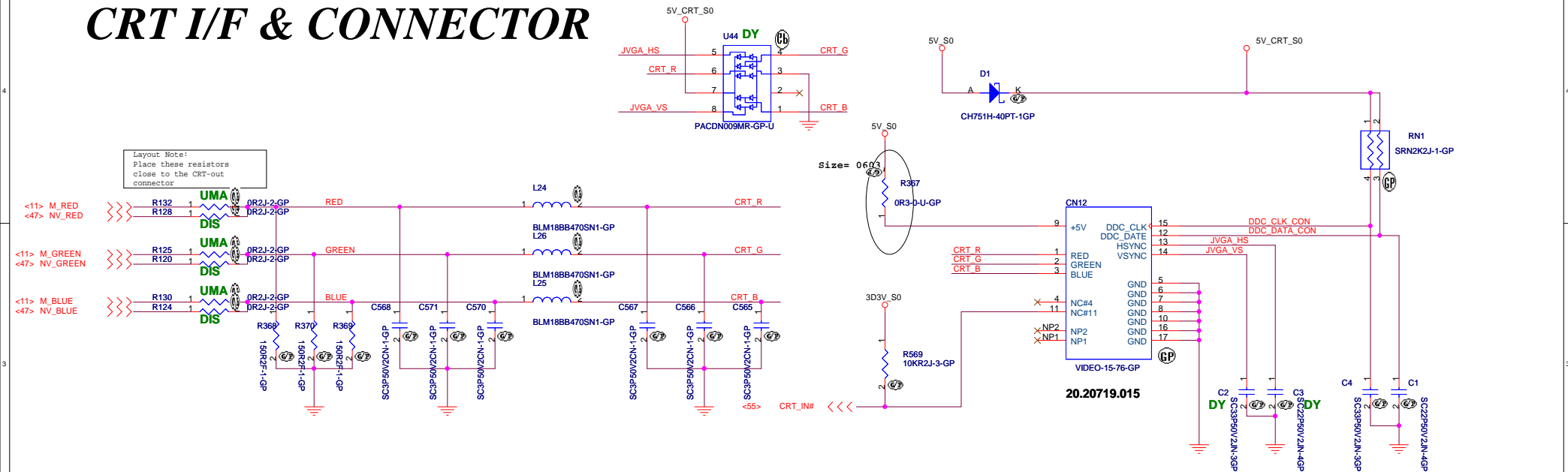
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"



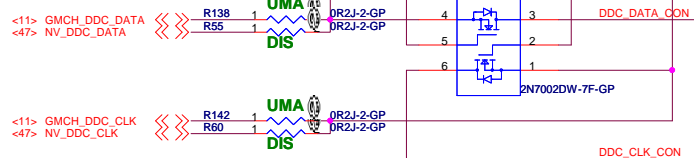
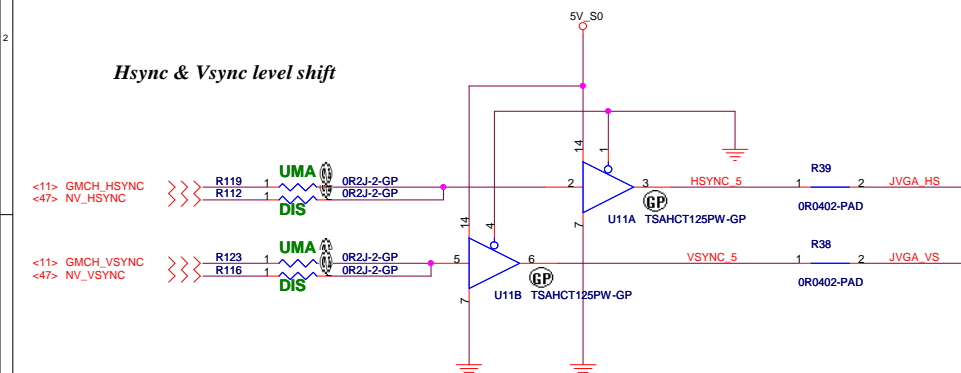
CRT I/F & CONNECTOR



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

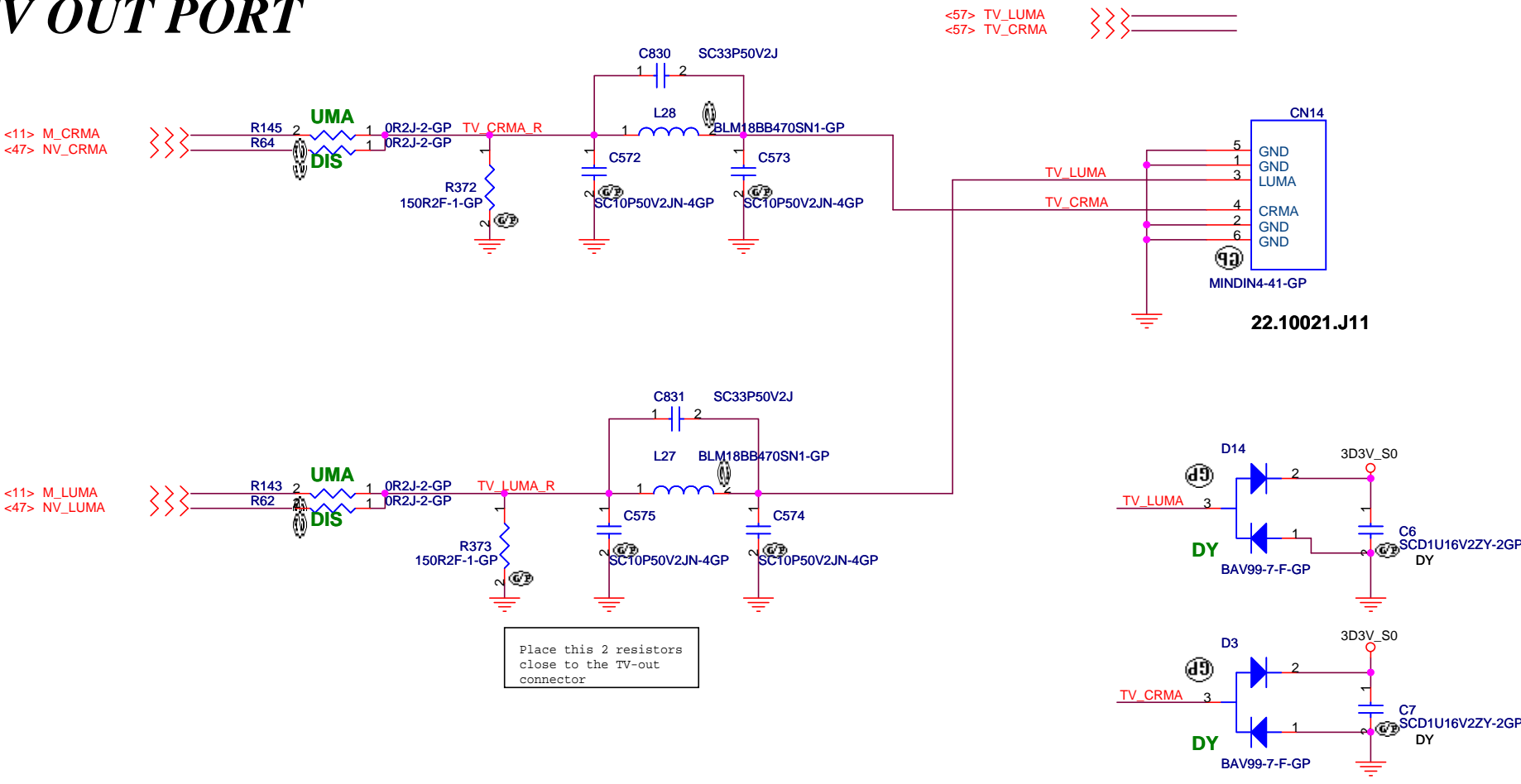
Hsync & Vsync level shift



A-NOTE2

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Title	
CRT Connector	
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TV OUT PORT



A-NOTE2

緯創資通

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Title

TV Connector

Size A4

Document Number

Anote2.0 INTEL

Rev -1

Date: Thursday, March 22, 2007

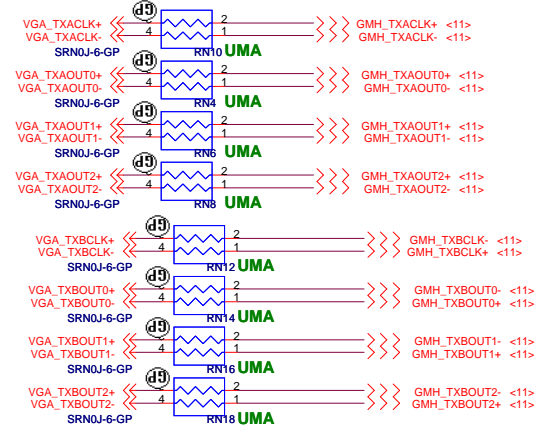
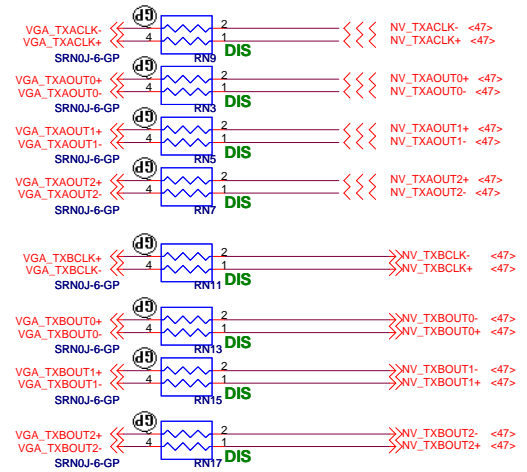
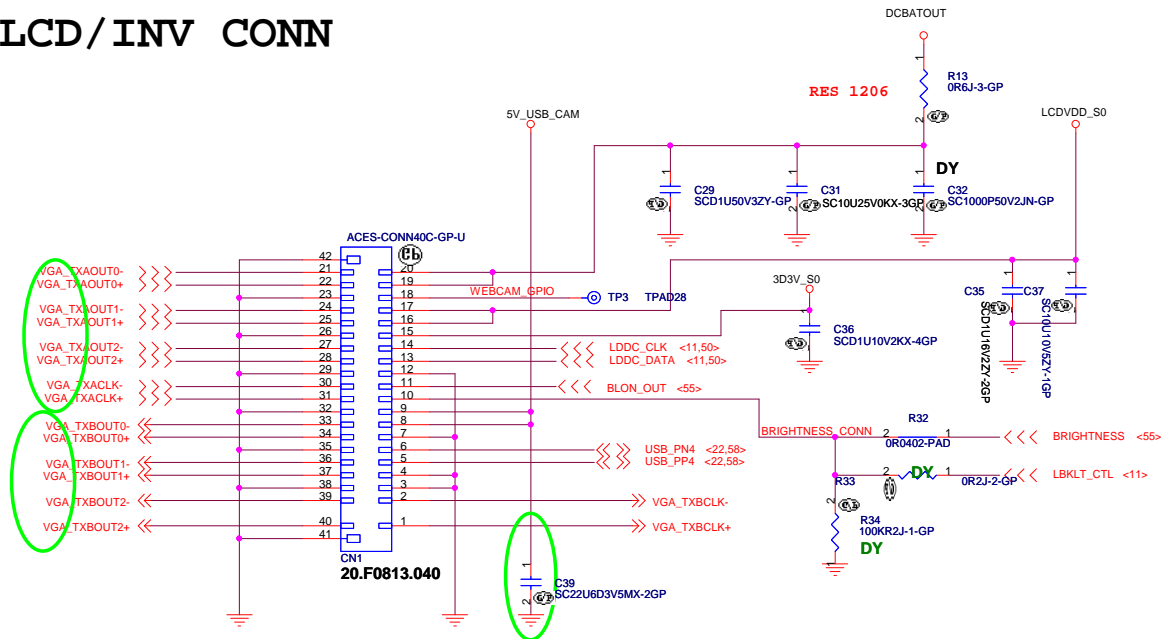
Sheet 18 of 56

LED / INVERTER INTERFACE

LCD/INV CONN

ATI LVDS INTERFACE

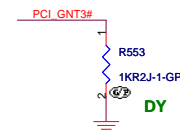
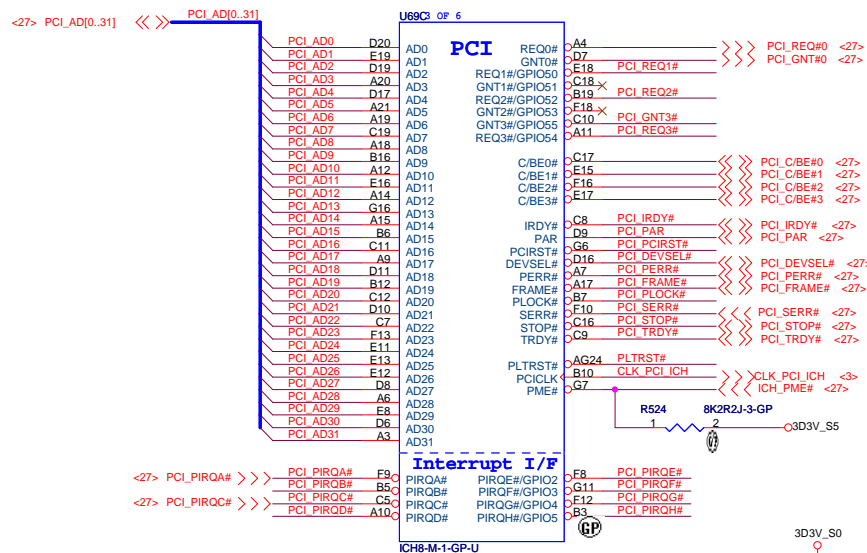
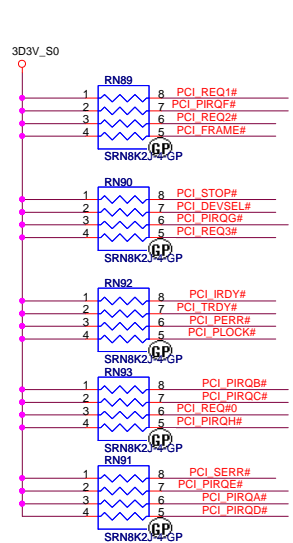
UMA LVDS INTERFACE



A-NOTE2

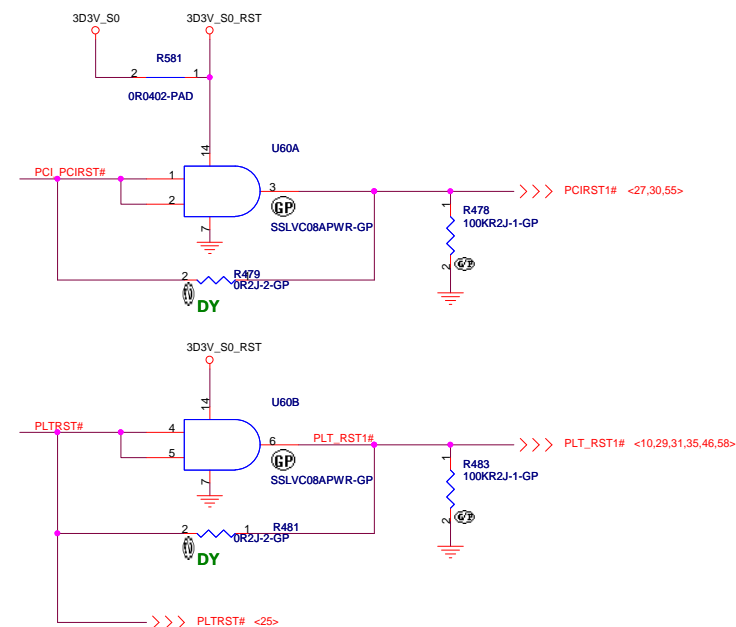
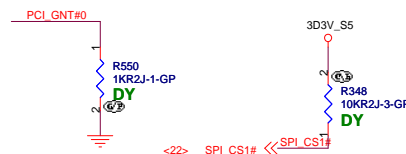
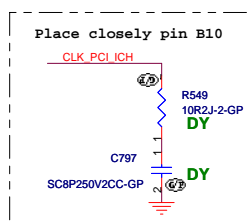
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

LCD/Inverter Connector			
Size A3	Document Number	Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet	19	of 56



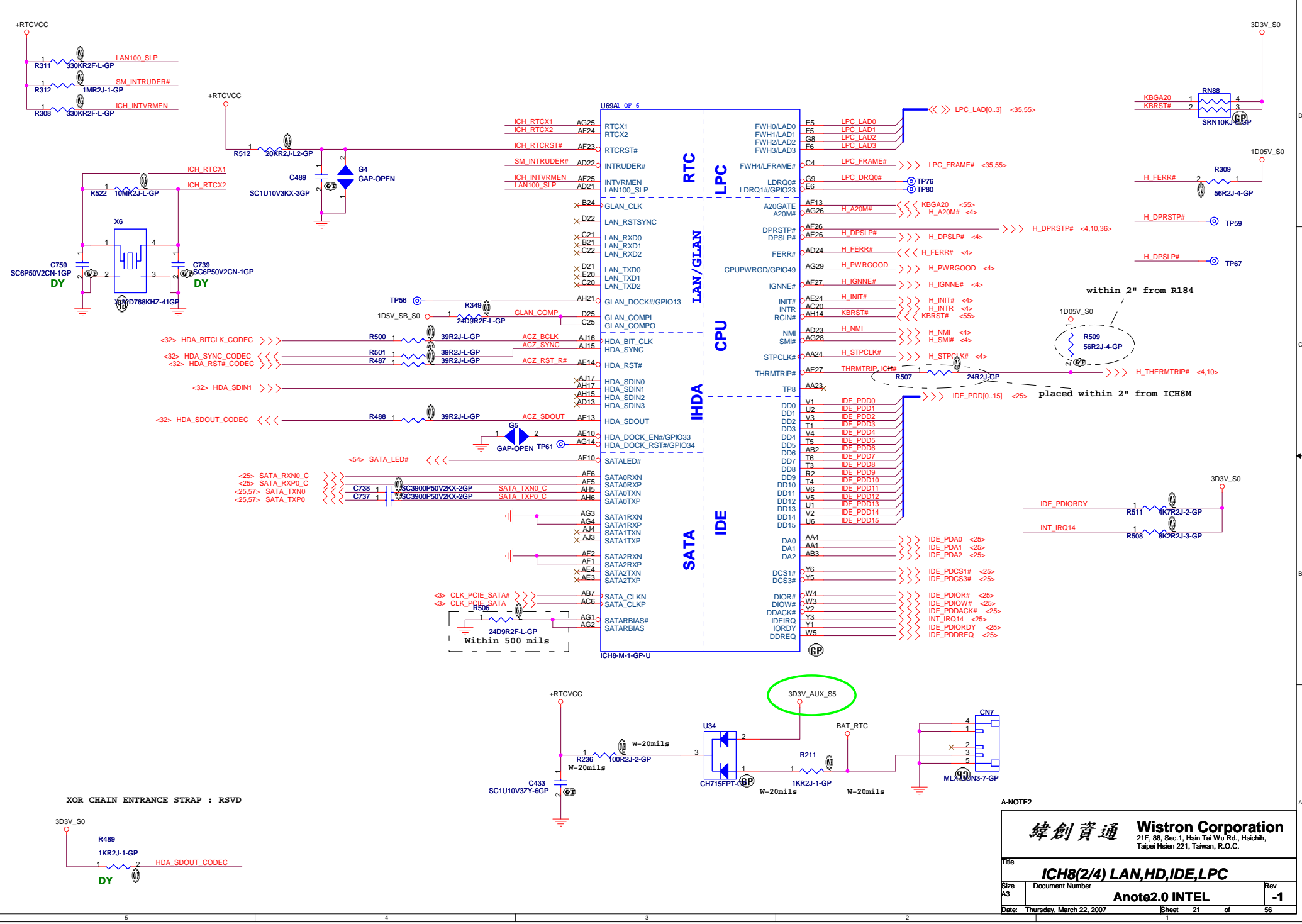
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH8(1/4)-PCI/INT
Size	Document Number
A3	Anot2.0 INTEL
Date: Thursday, March 22, 2007	Sheet 20 of 56



A-NOTE2

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ICH8(2/4) LAN,HD,IDE,LPC		
Size A3	Document Number	Rev -1
Date: Thursday, March 22, 2007		

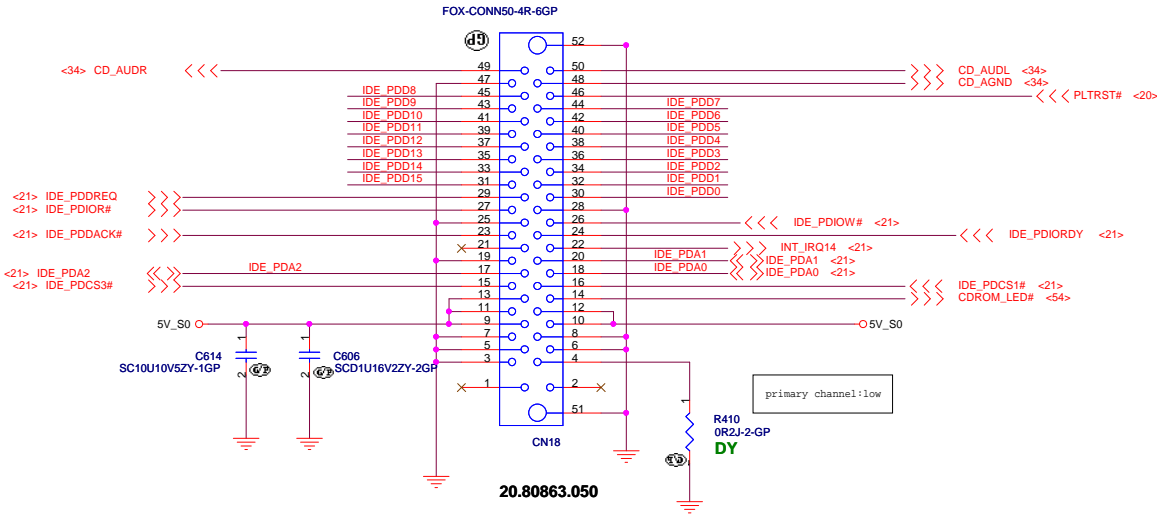




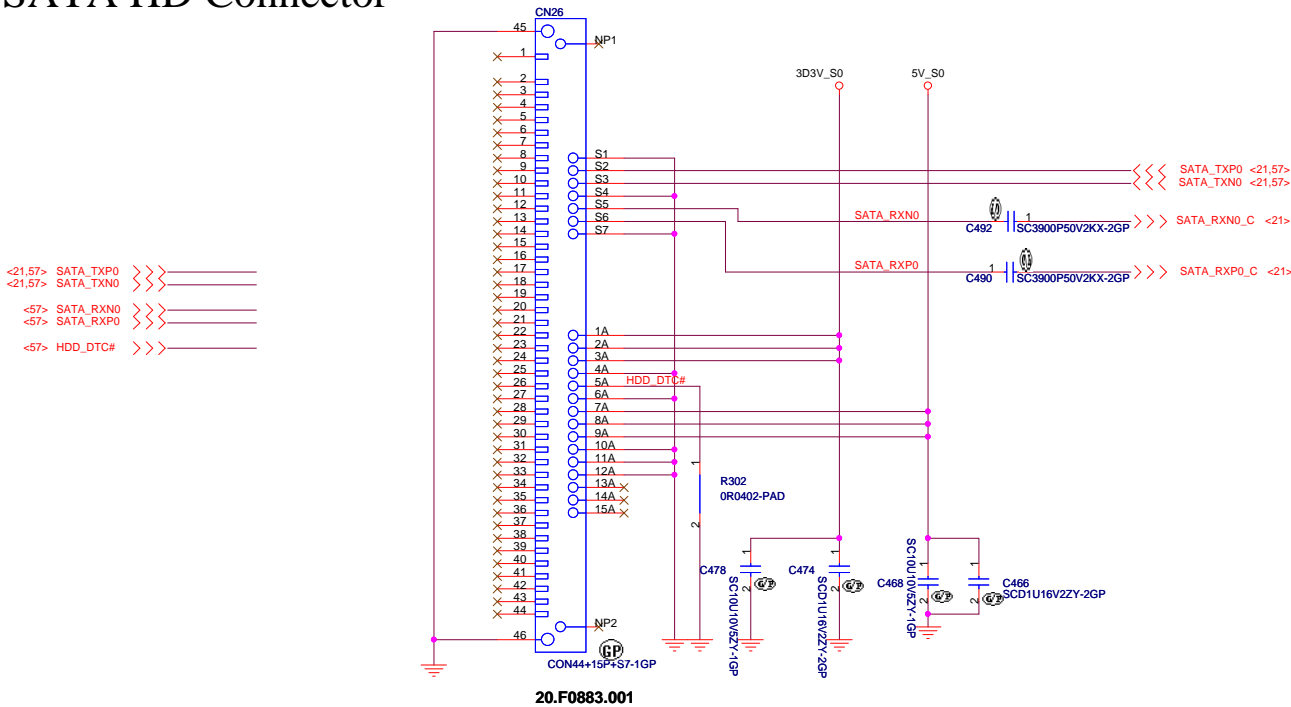
CD-ROM CONNECTOR

Lab1 20.80346.050
Lab2 20.80863.050

<<< IDE_PDD[0..15] <21>



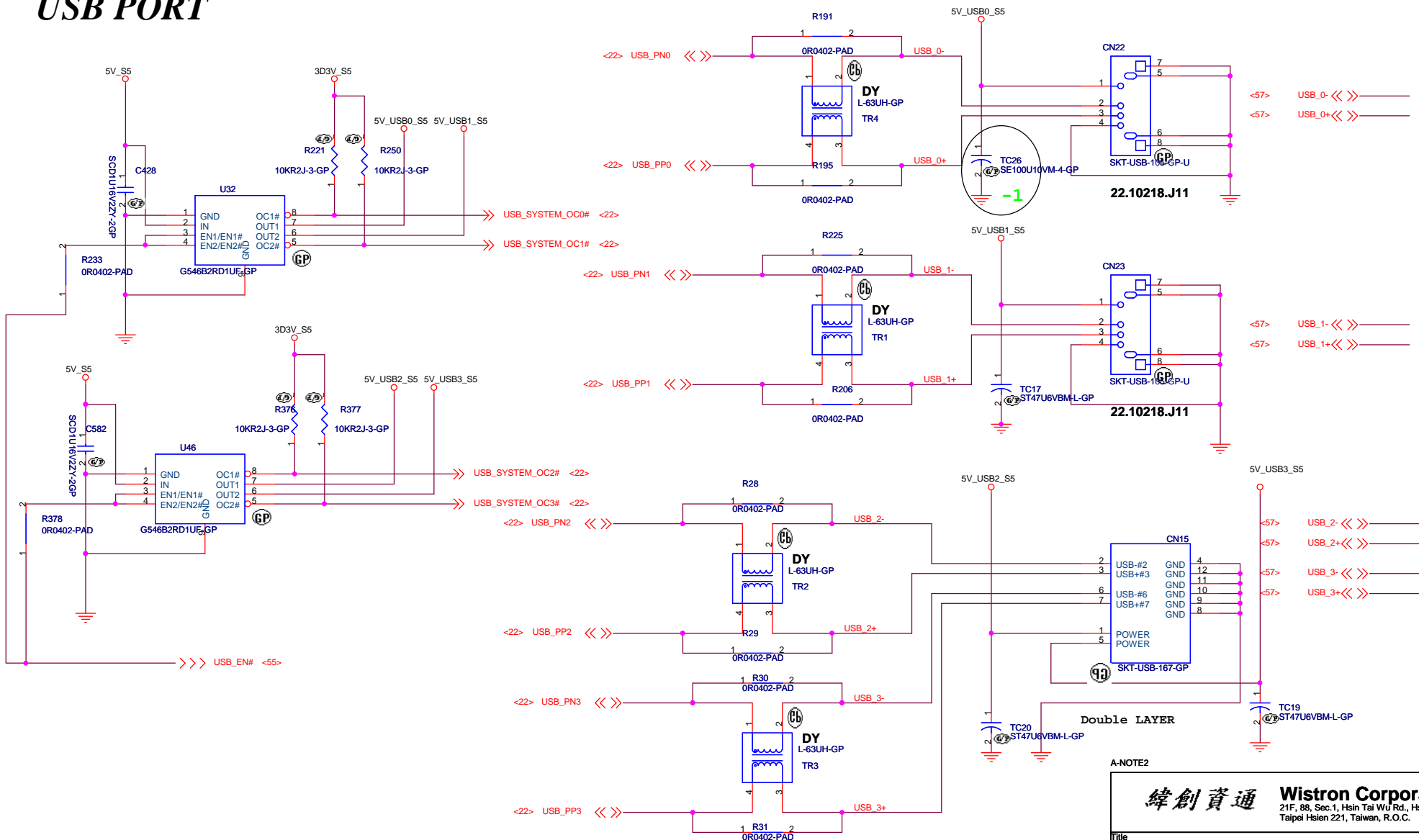
SATA HD Connector



A-NOTE2

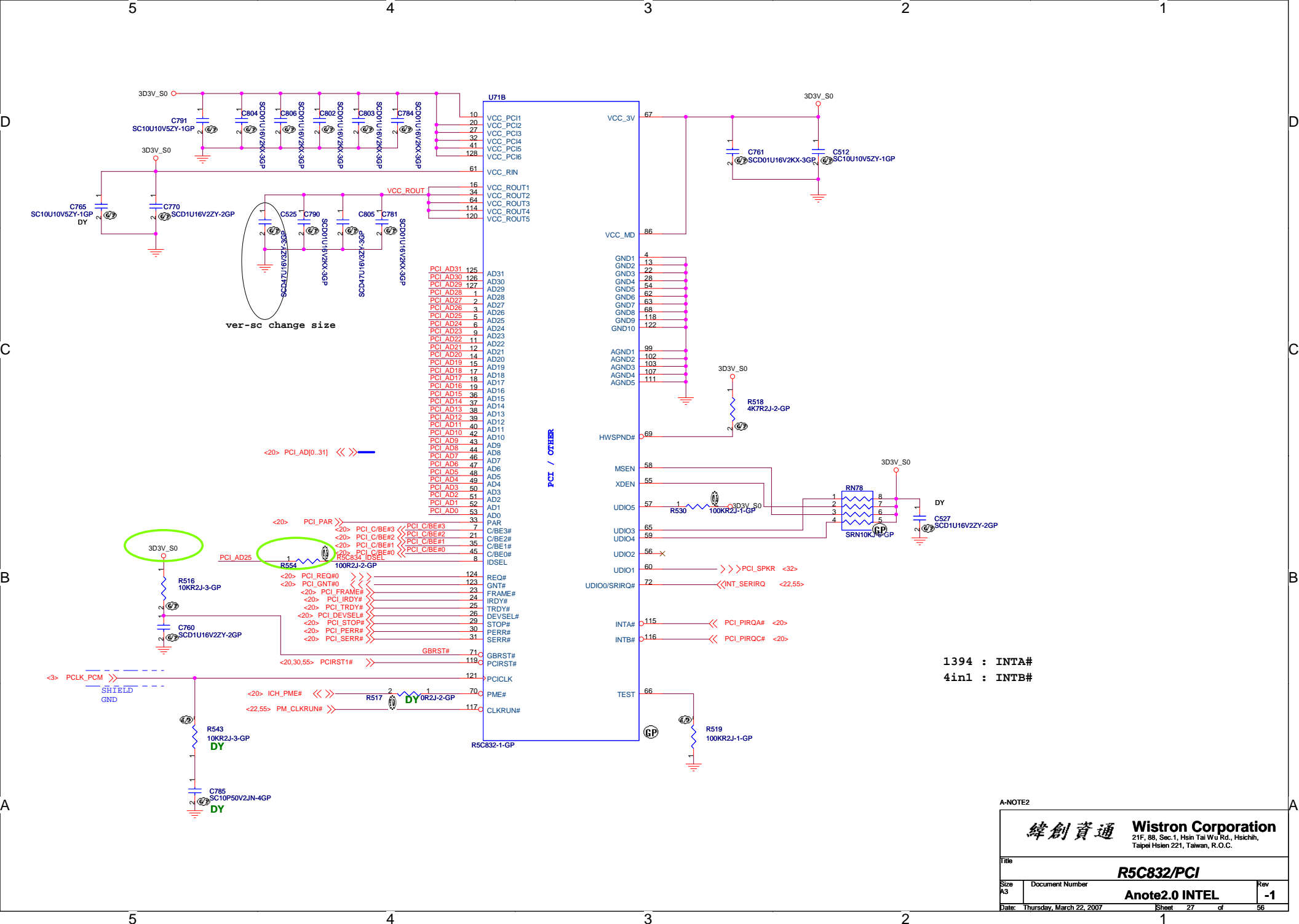
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HD/CDROM/USB	
Size	Document Number
A3	Anote2.0 INTEL
Date:	Thursday, March 22, 2007
Sheet	25 of 56
Rev	-1

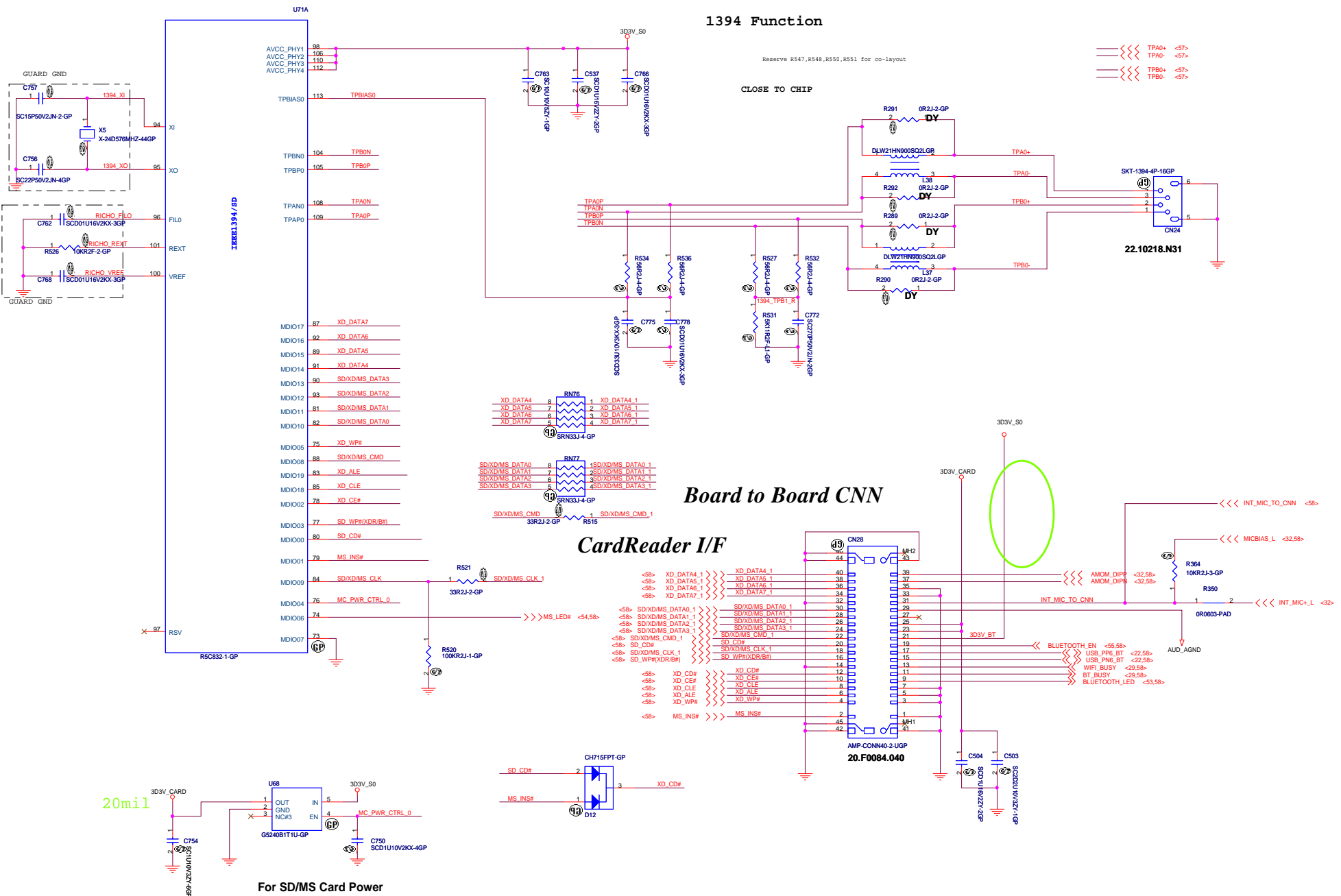
USB PORT



A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB I/O	
Title Size B Date: Thursday, March 22, 2007	Document Number Anote2.0 INTEL Sheet 26 of 56
Rev -1	





A-NOTE2

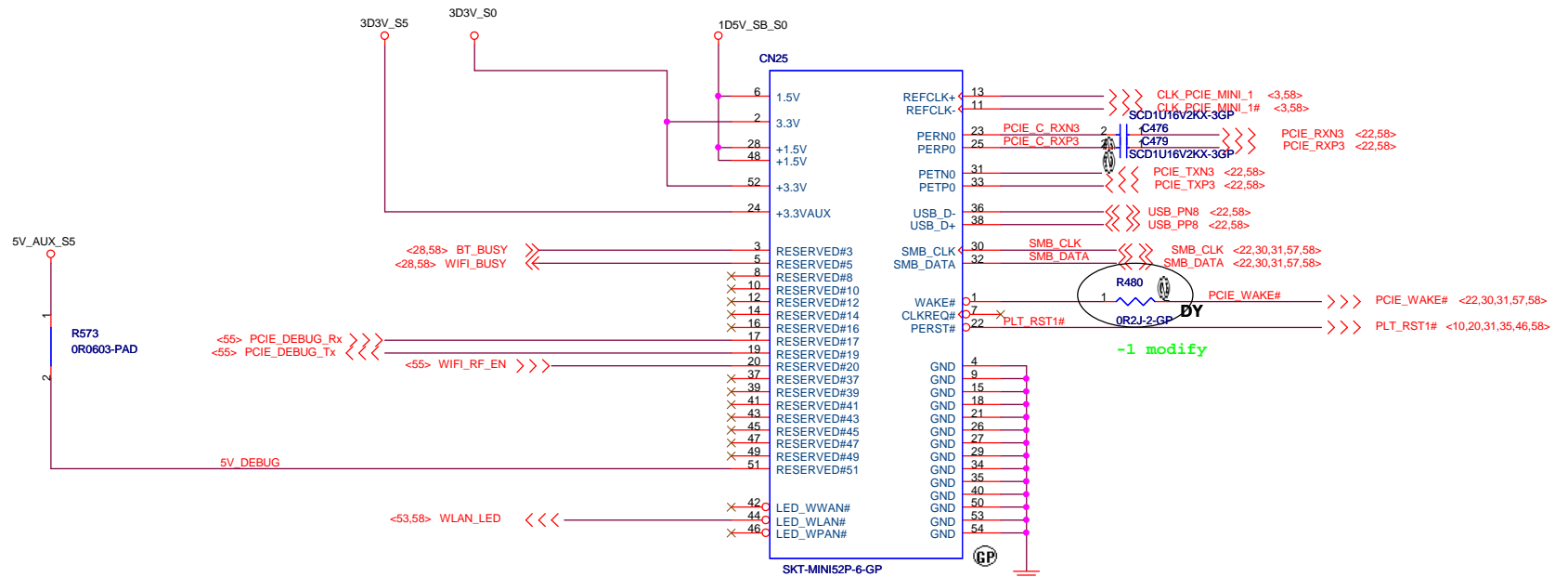
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, Taiwan, R.O.C.

R5C832/IEEE1394/SD		
Size	Document Number	Rev
C	Anote2.0 INTEL	-1
Date:	Thursday, March 22, 2007	Sheet 28 of 58

Mini PCI-E Connector

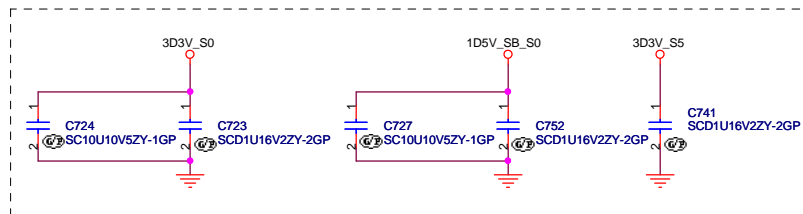
Port-1

Only port-1 support USB



62.10043.261

Note: 9/5 ME update



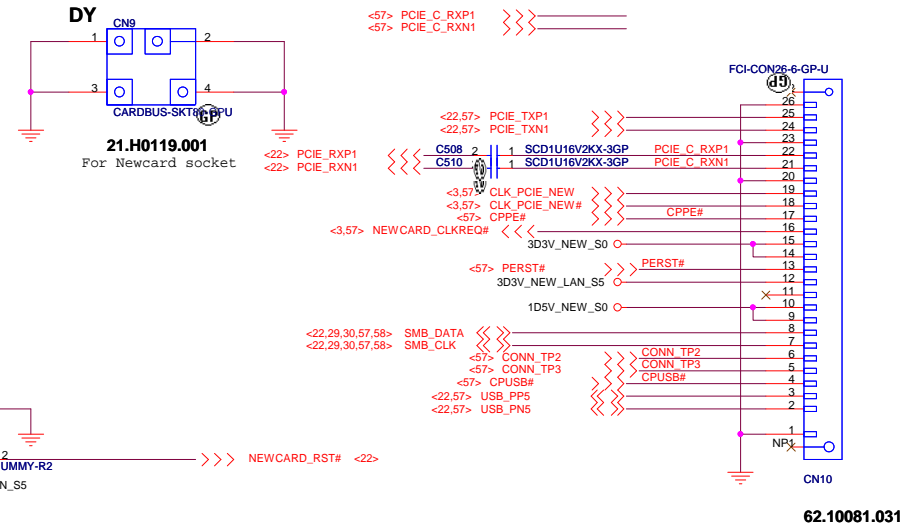
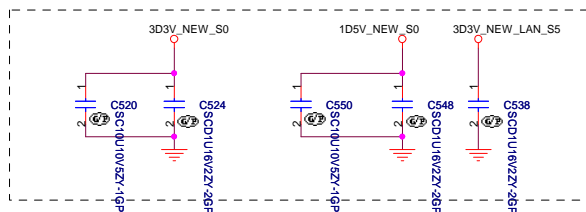
A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI CARD CONN.	
Title Size B Date: Thursday, March 22, 2007	Document Number Anote2.0 INTEL Sheet 29 of 56
Rev -1	

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



Place them Near to Connector

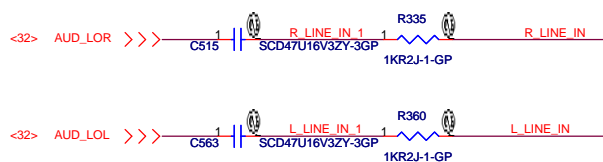
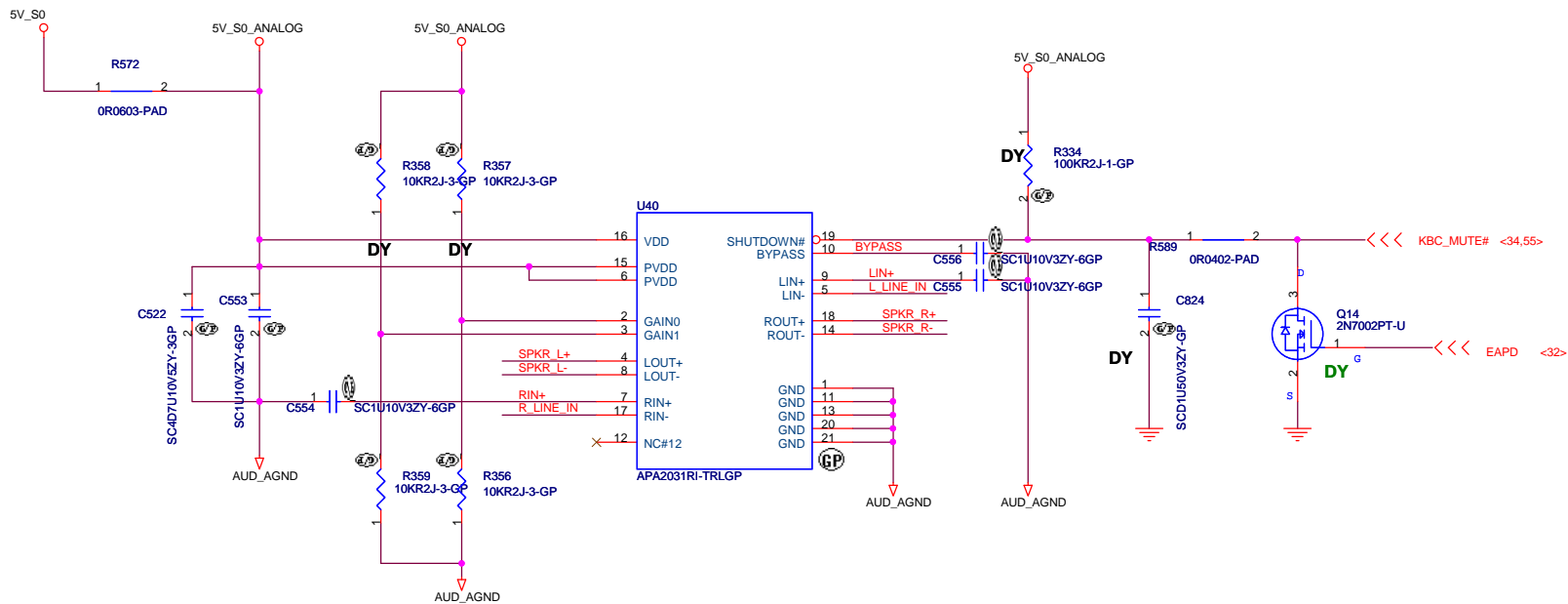


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

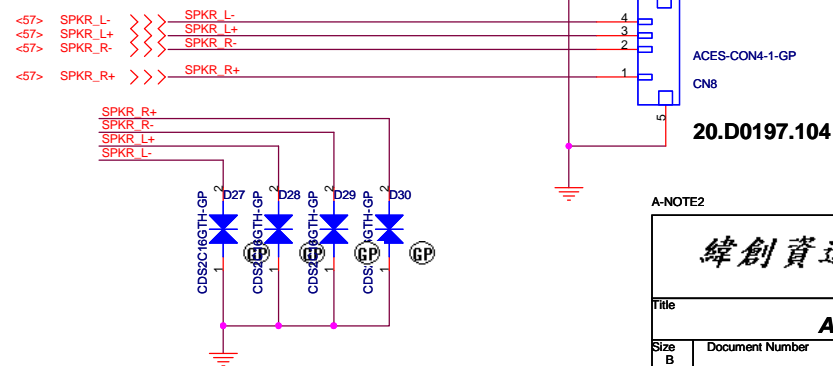
Title	LAN connector/NEW CARD/SIM
-------	-----------------------------------

Size A3	Document Number Anote2.0 INTEL	Rev -1
Date: Thursday, March 22, 2007	Sheet 31 of 56	





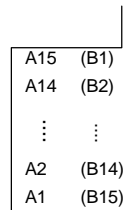
Speaker



A-NOTE2

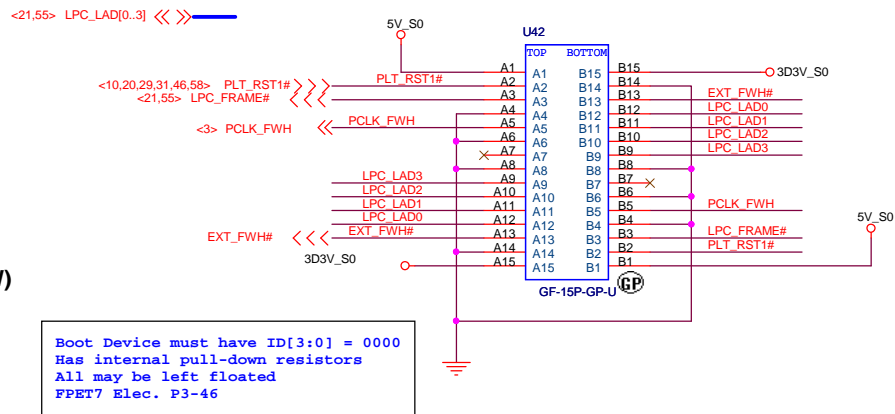
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
AUDIO AMP/SPEAKER		
Size B	Document Number	Rev
	Anote2.0 INTEL	-1
Date: Thursday, March 22, 2007	Sheet 33	of 56

TOP VIEW

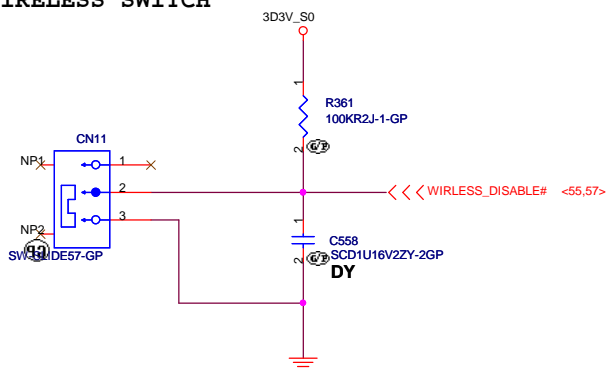


(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

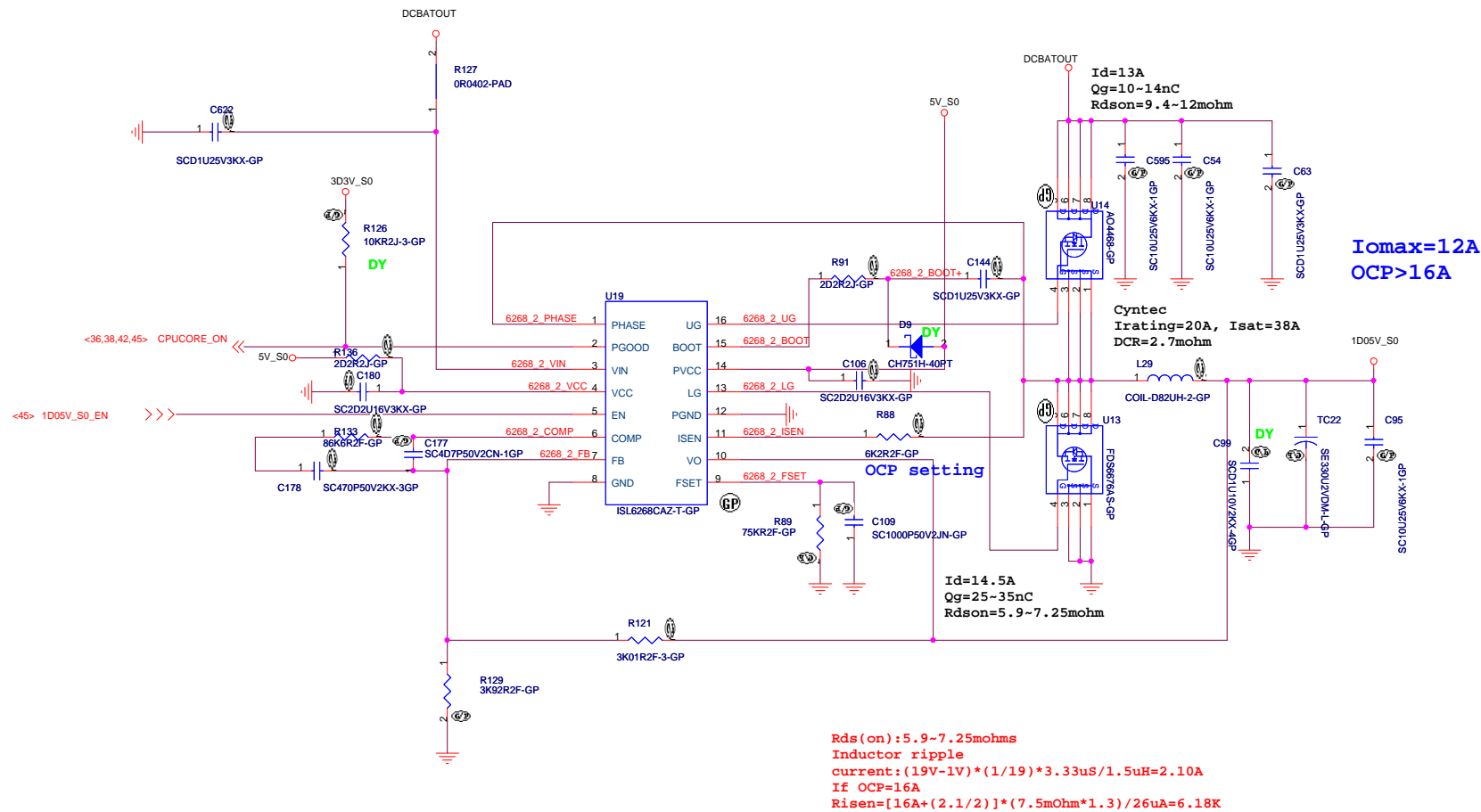


WIRELESS SWITCH



A-NOTE2

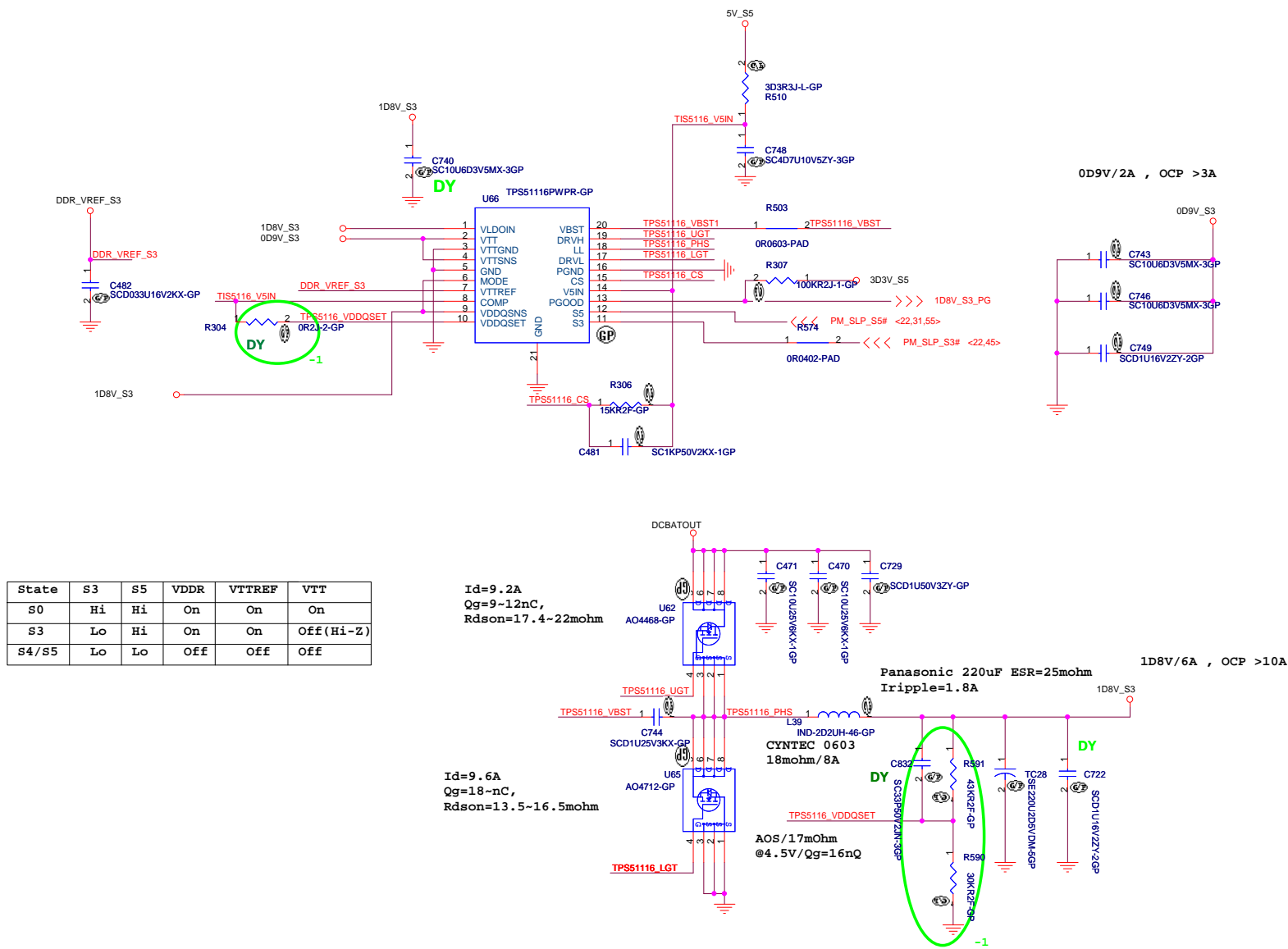
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>FWH and Debug</i>			
Size B	Document Number		Rev -1
Anote2.0 INTEL			
Date:	Thursday, March 22, 2007	Sheet 35 of 56	



A-NOTE2

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05V S0 ISL6268			
Size A3	Document Number		Rev -1
Date: Thursday, March 22, 2007		Sheet 39 of 56	Anote2.0 INTEL

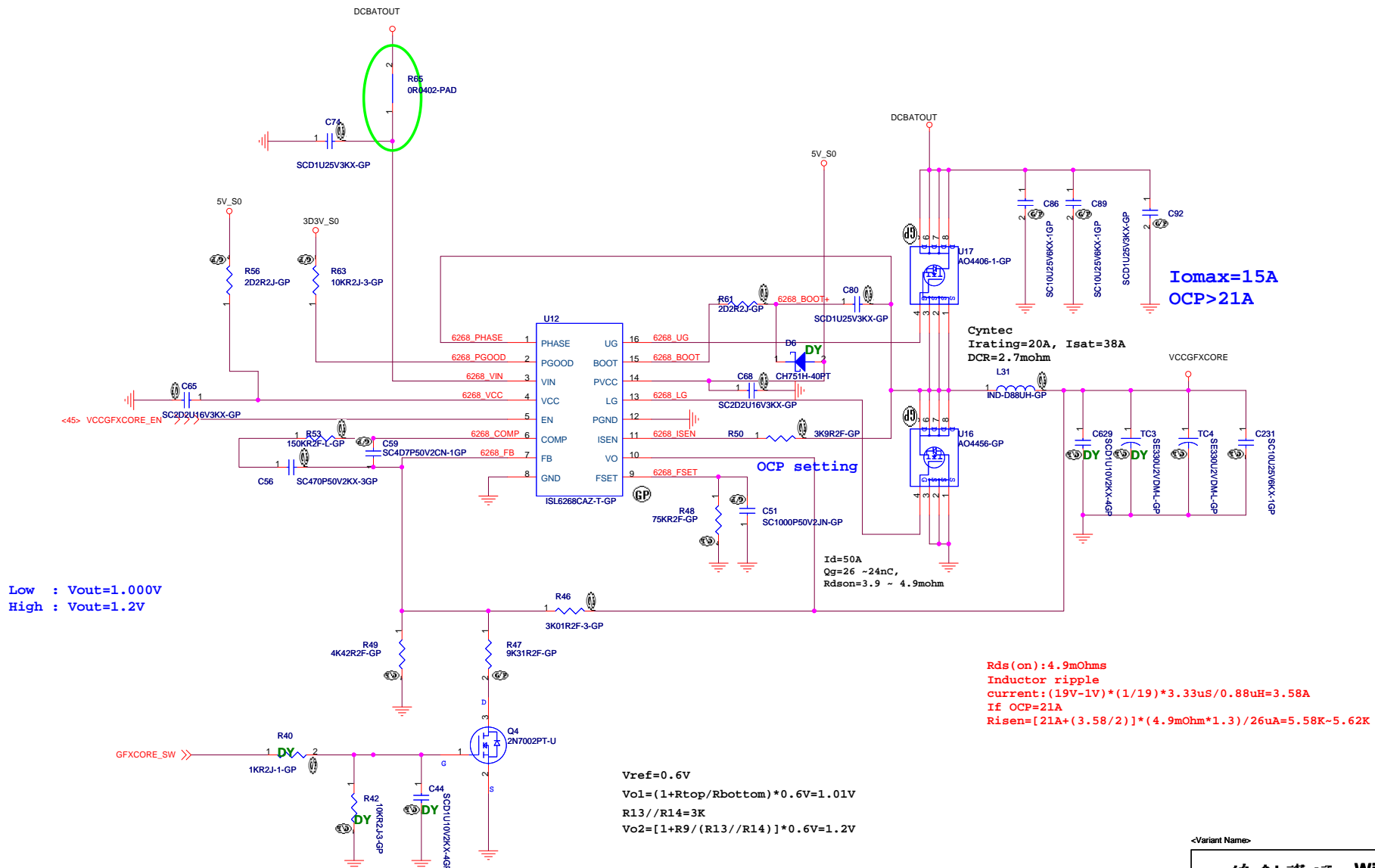
TI TPS51116 for 1D8V and 0D9V



A-NOTE2

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
TPS51116 1D8V/0D9V		
Size	Document Number	Rev
A3	Anote2.0 INTEL	-1
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reserve for cost down

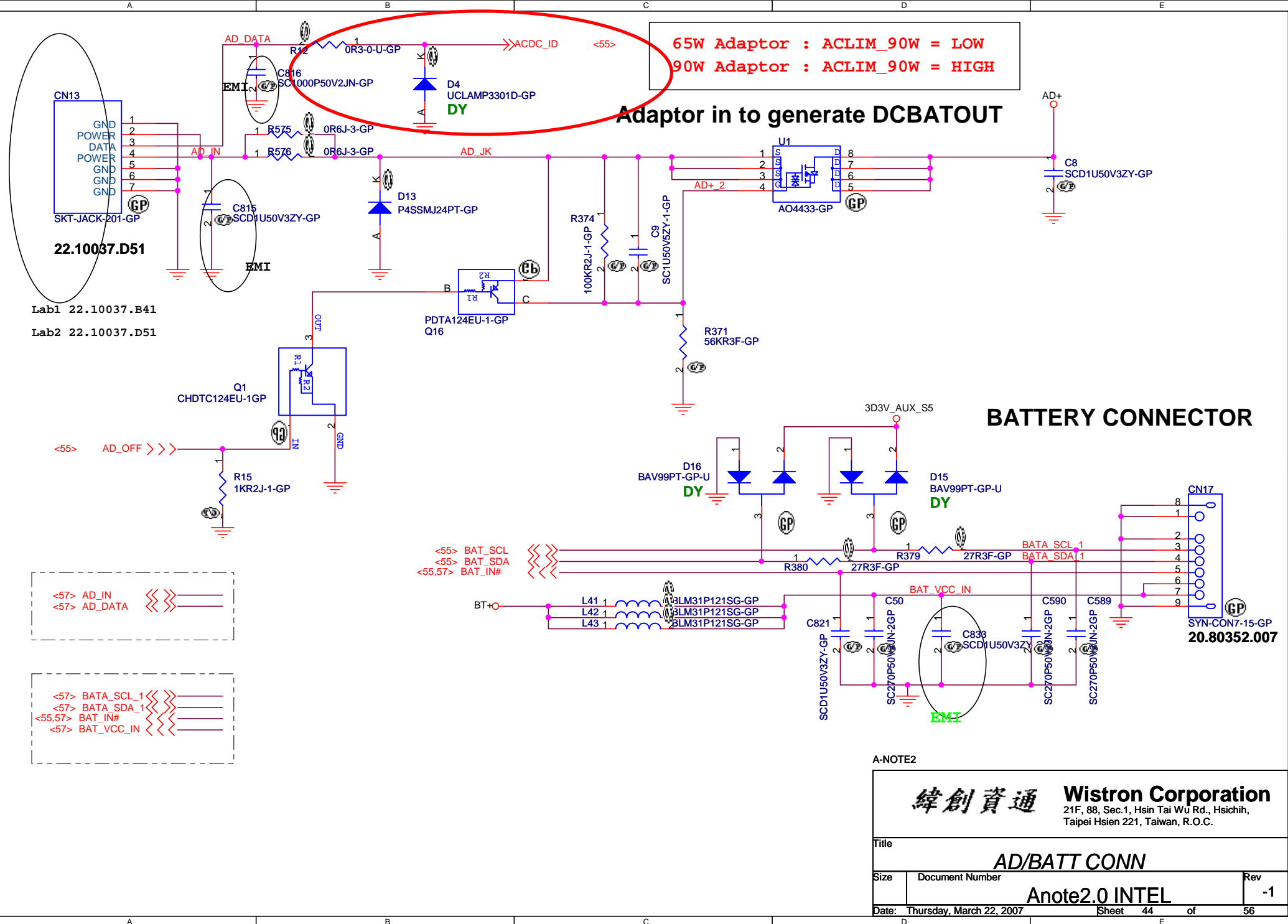


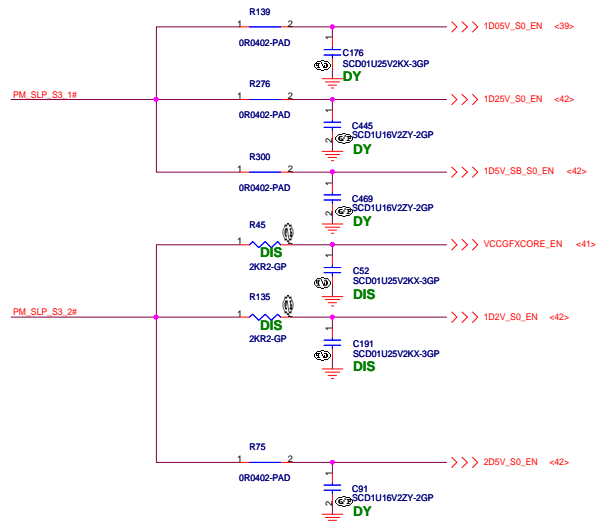
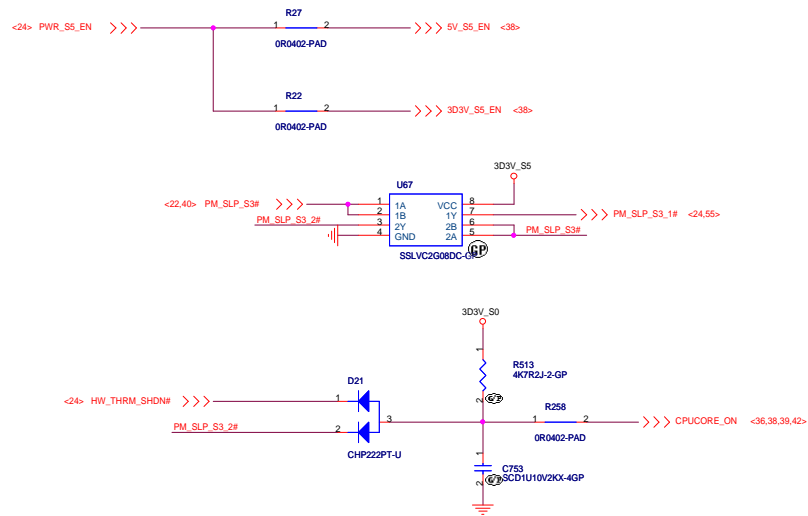
Vo_Select	Hi	Lo
Vout	1.2V	1.01V

<Variant Name>

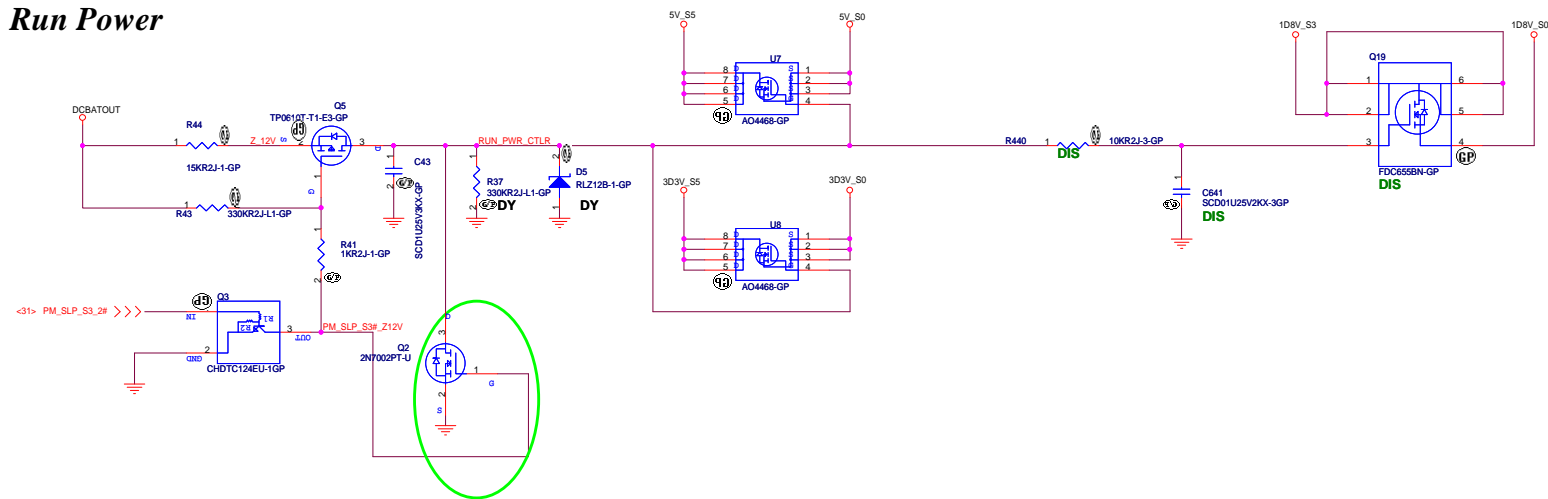
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DC/DC VCCGFXCORE (ISL6268)	
Title Size A3 Date: Thursday, March 22, 2007	Document Number Anote2.0 INTEL Sheet 41 of 56
Rev -1	





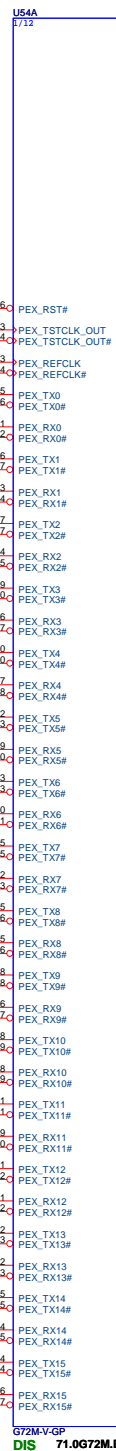


Run Power

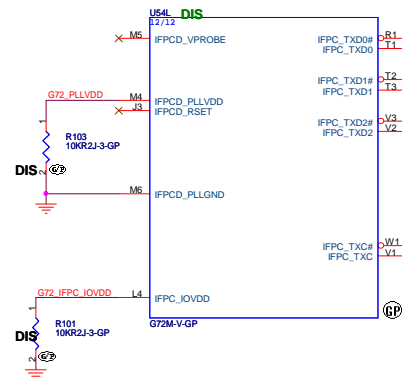
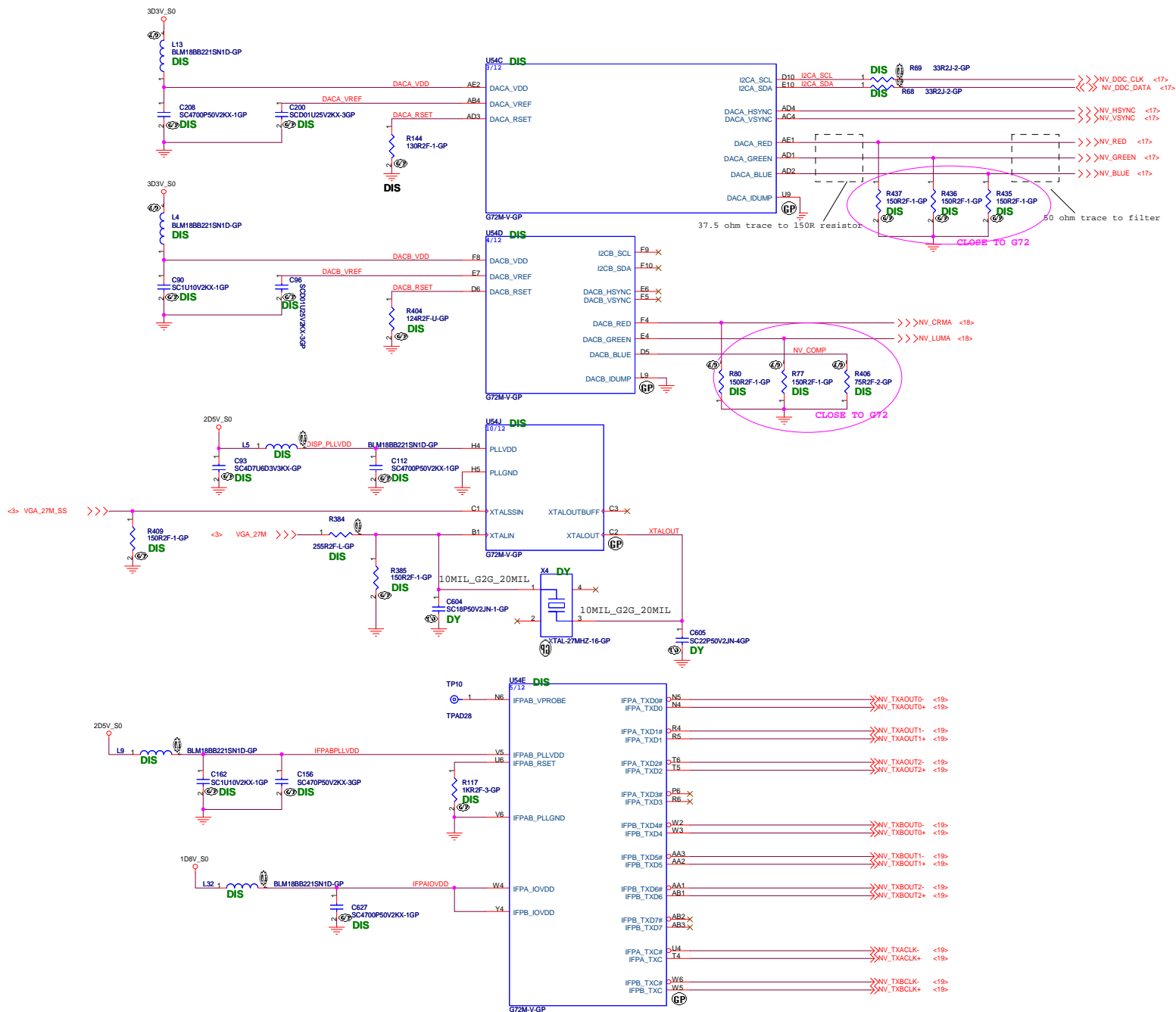


A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
PWRPLANE&RESET LOGIC		
Size C	Document Number	Rev -1
Date: Thursday, March 22, 2007	Sheet 45 of 56	

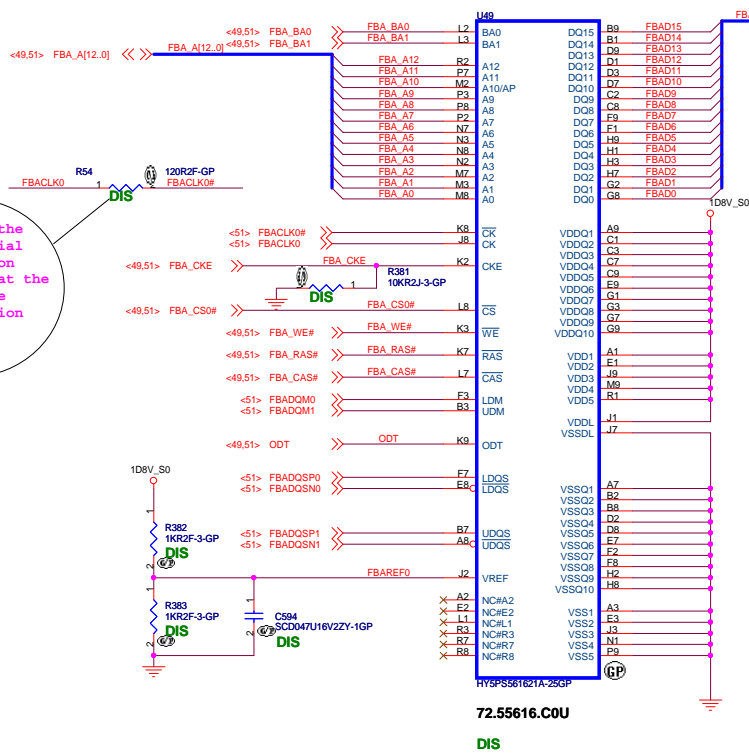


Title				G72M PCIE			
Size		Document Number					Rev
		Anote2.0 INTEL					-1
Date: Thursday, March 22, 2007			Sheet 46		of 56		

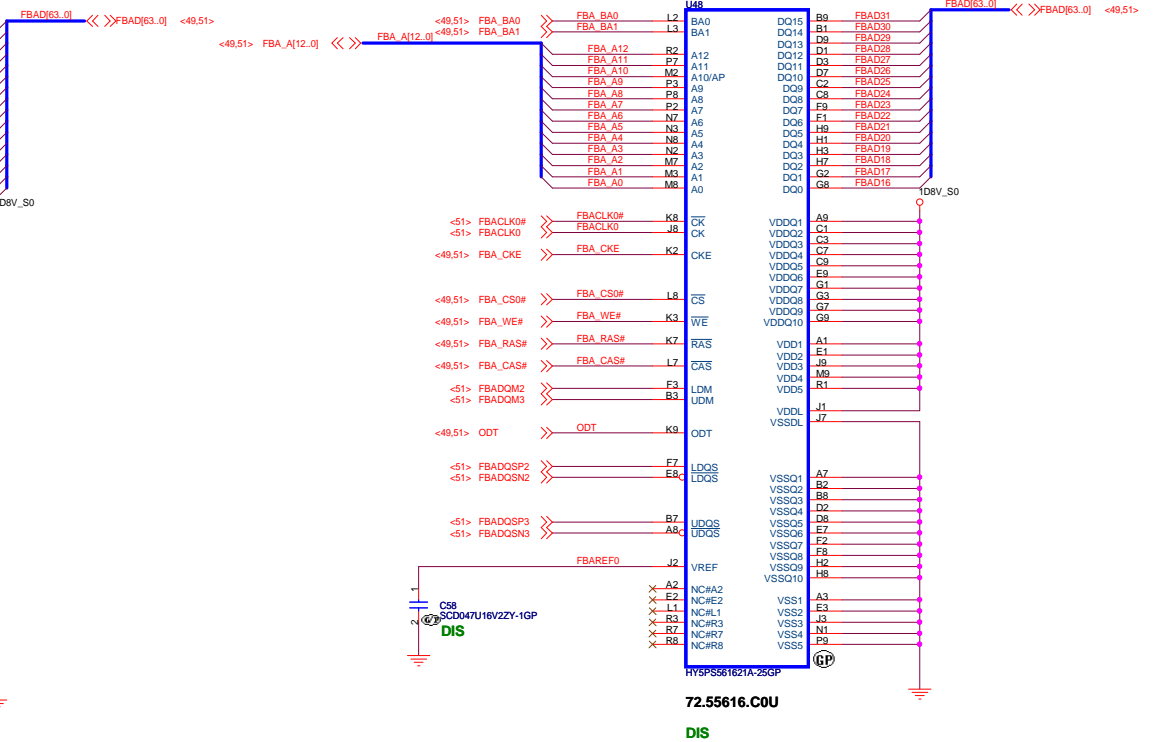
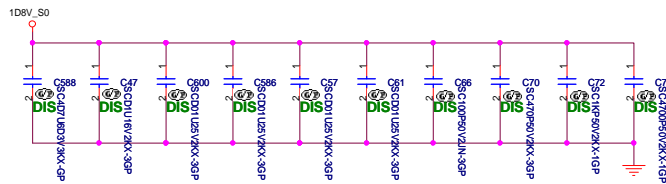


A-NOTE2		緯創資通 Wistron Corporation 21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File		G72M CRT & TV OUT	
Size	Document Number	Anote2.0 INTEL	Rev -1
Date	Thursday, March 22, 2007	Sheet 47	of 56

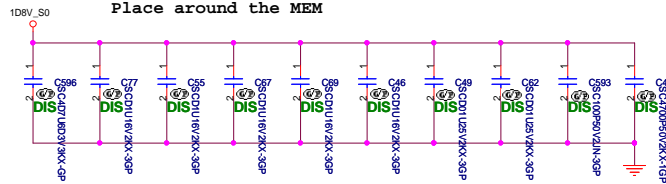
* "Place the differential termination resistor at the end of the transmission line"



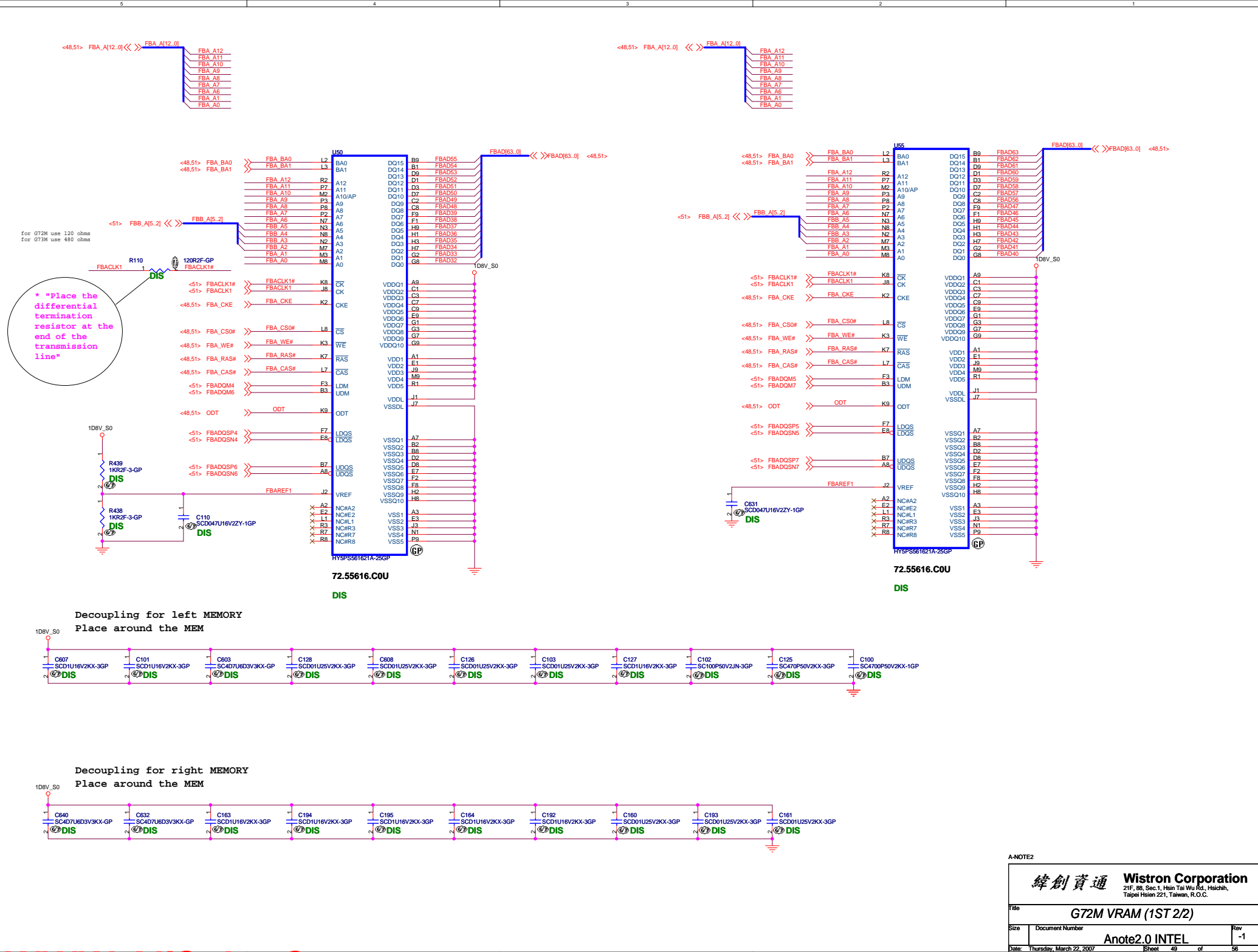
Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



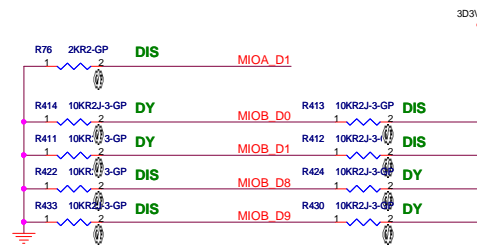
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)



STRAPS, Mechanical Parts

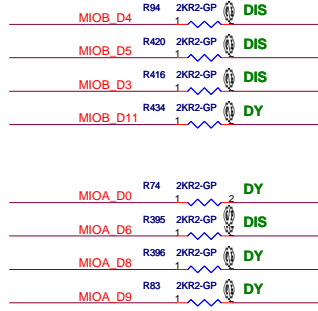
Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



<50> MIOA_D0 << MIOA_D0
<50> MIOA_D1 << MIOA_D1
<50> MIOA_D6 << MIOA_D6
<50> MIOA_D8 << MIOA_D8
<50> MIOA_D9 << MIOA_D9

<50> MIOB_D0 << MIOB_D0
<50> MIOB_D1 << MIOB_D1
<50> MIOB_D3 << MIOB_D3
<50> MIOB_D4 << MIOB_D4
<50> MIOB_D5 << MIOB_D5
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00

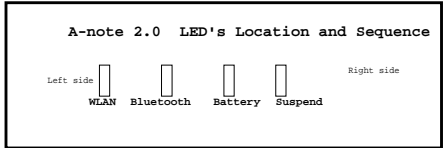
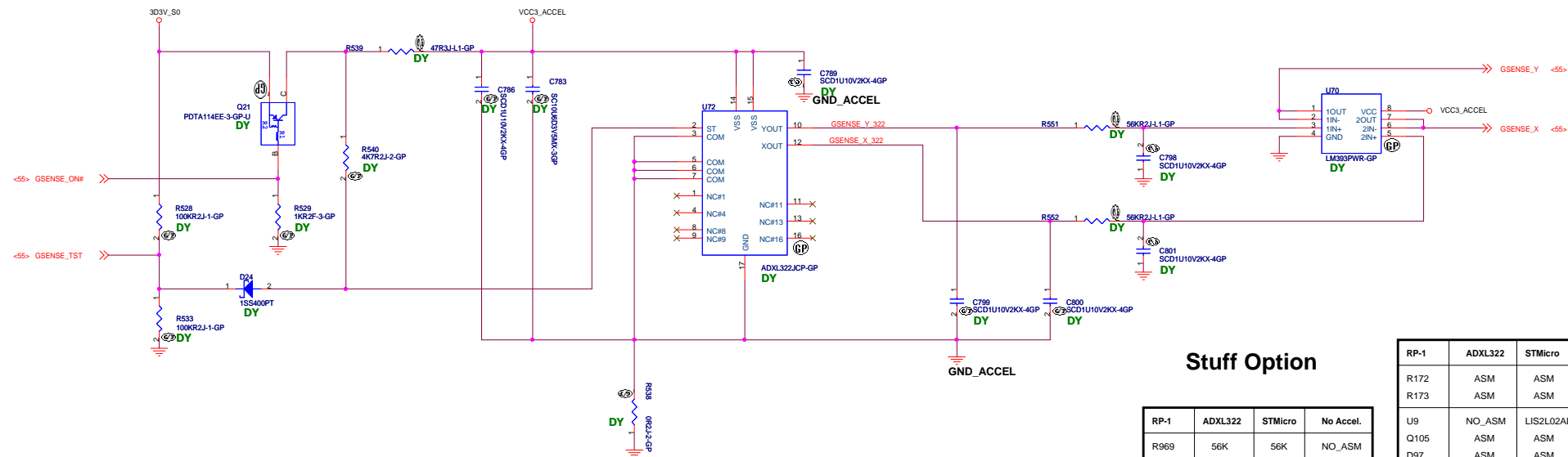
Bit Signal	Values
MIOA_D1: SUB_VENDOR	0 NO BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0]	Config	FB Bus Width	Definitions
RAM_CFG[3..0]			
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

MIOB_D4: PCI_DEVID_0	
MIOB_D5: PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3: PCI_DEVID_2	
MIOB_D11: PCI_DEVID_3	0111 G72MV G72MZ=6 ,G73=8

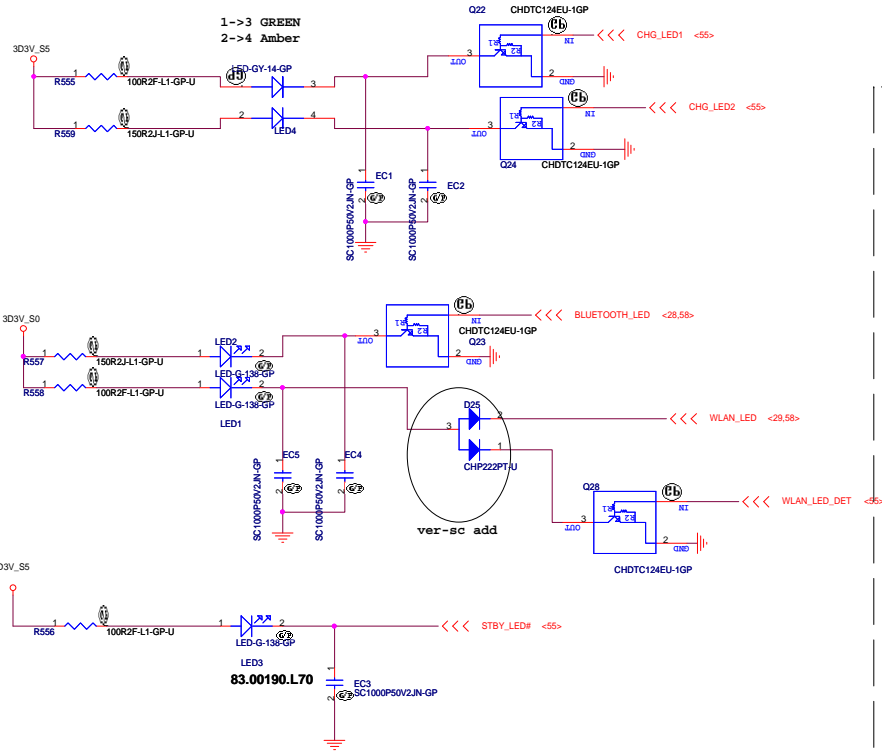
MIOA_D0: PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT



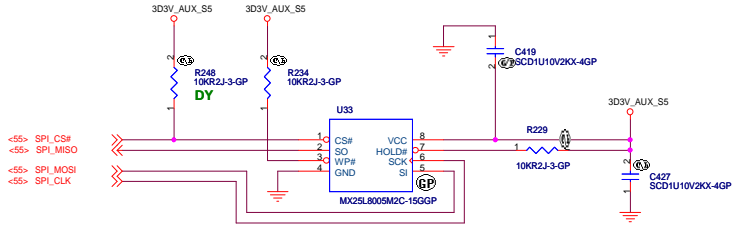
Stuff Option

RP-1	ADXL322	STMico	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

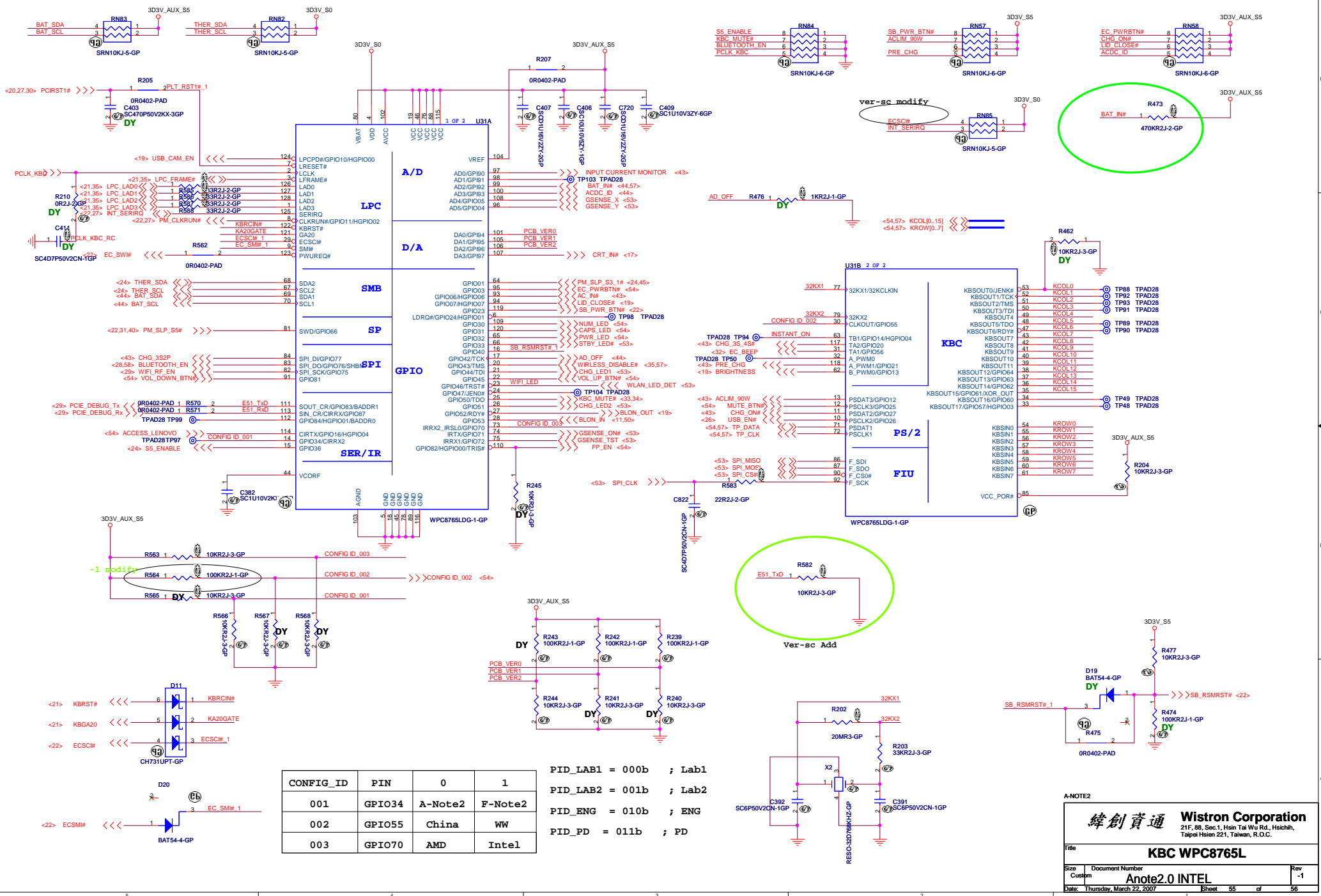
RP-1	ADXL322	STMico	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

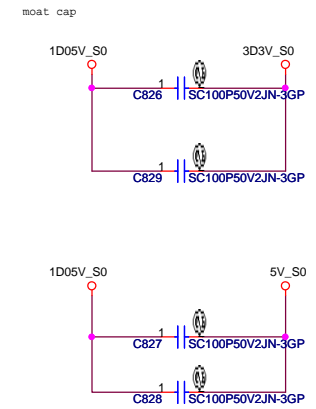
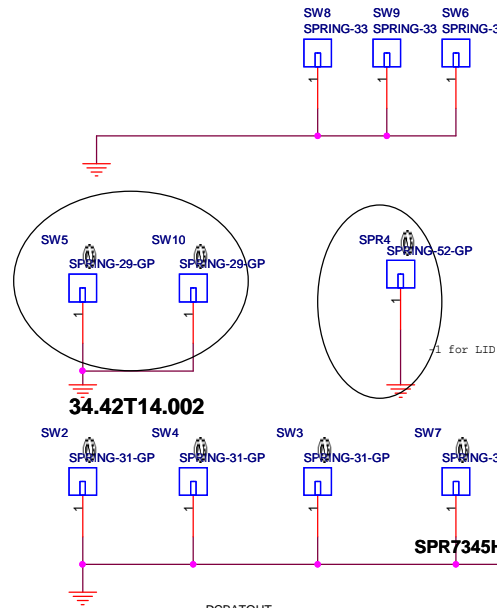
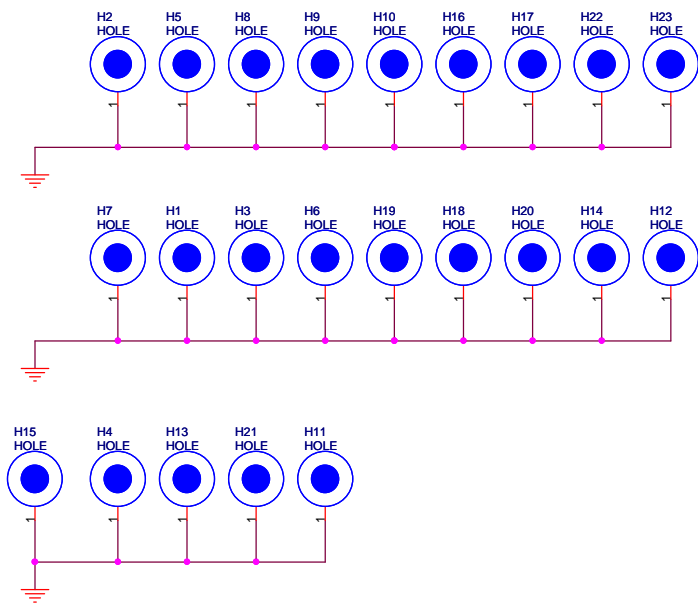


SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01





34.42T14.002

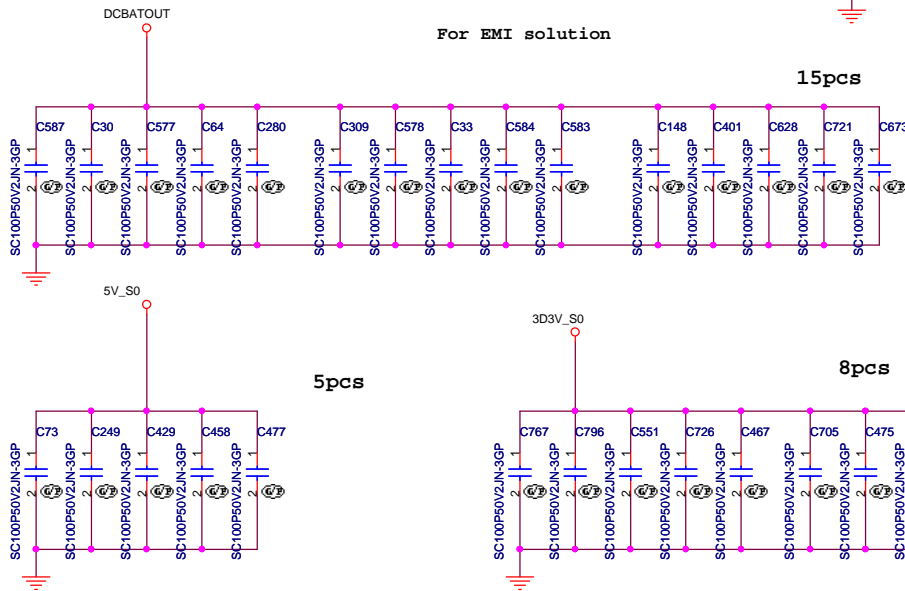
SPR7345H154

For EMI solution

15pcs

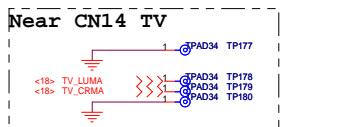
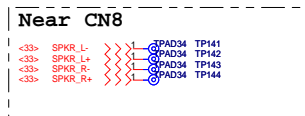
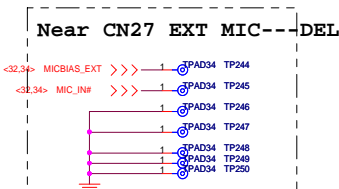
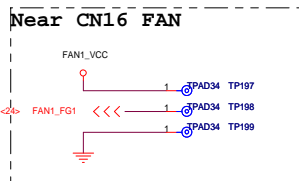
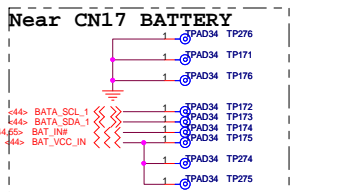
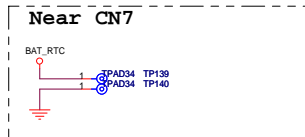
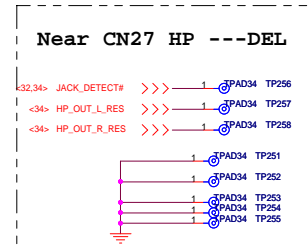
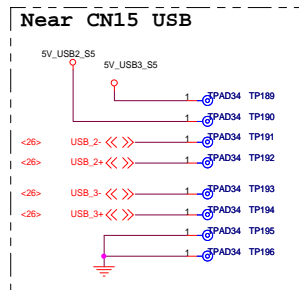
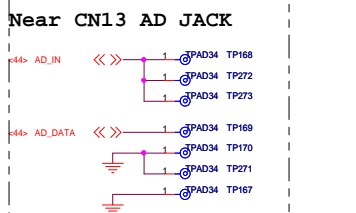
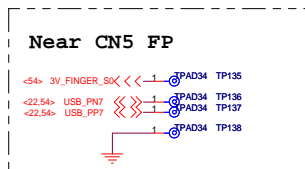
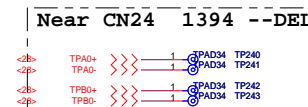
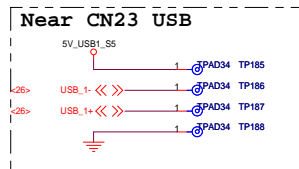
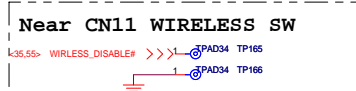
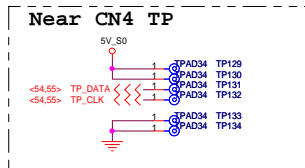
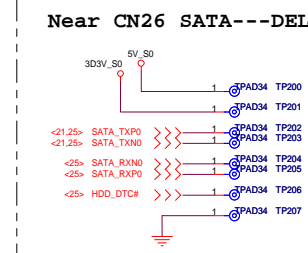
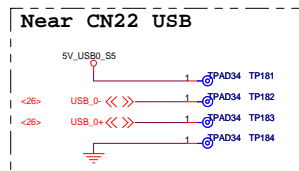
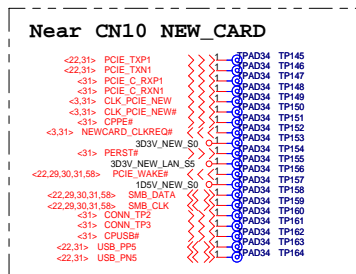
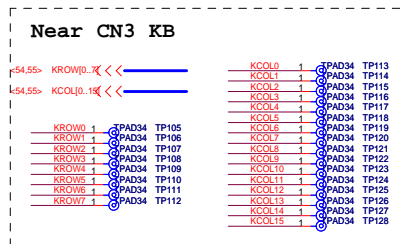
EMI LAB2 add

ver-sc add

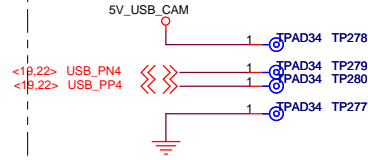


A-NOTE2

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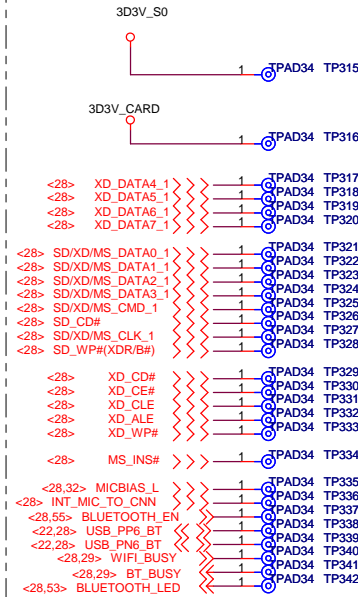
Near LCD CNN--CAM



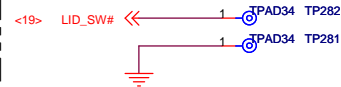
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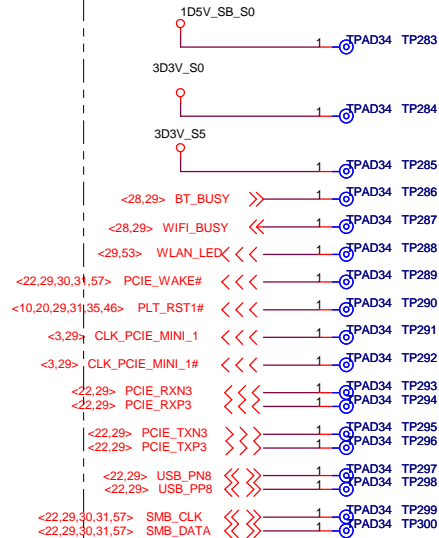
Daughter-BD



Near SW1



Near CN25--Mini -PCIE



A-NOTE2

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